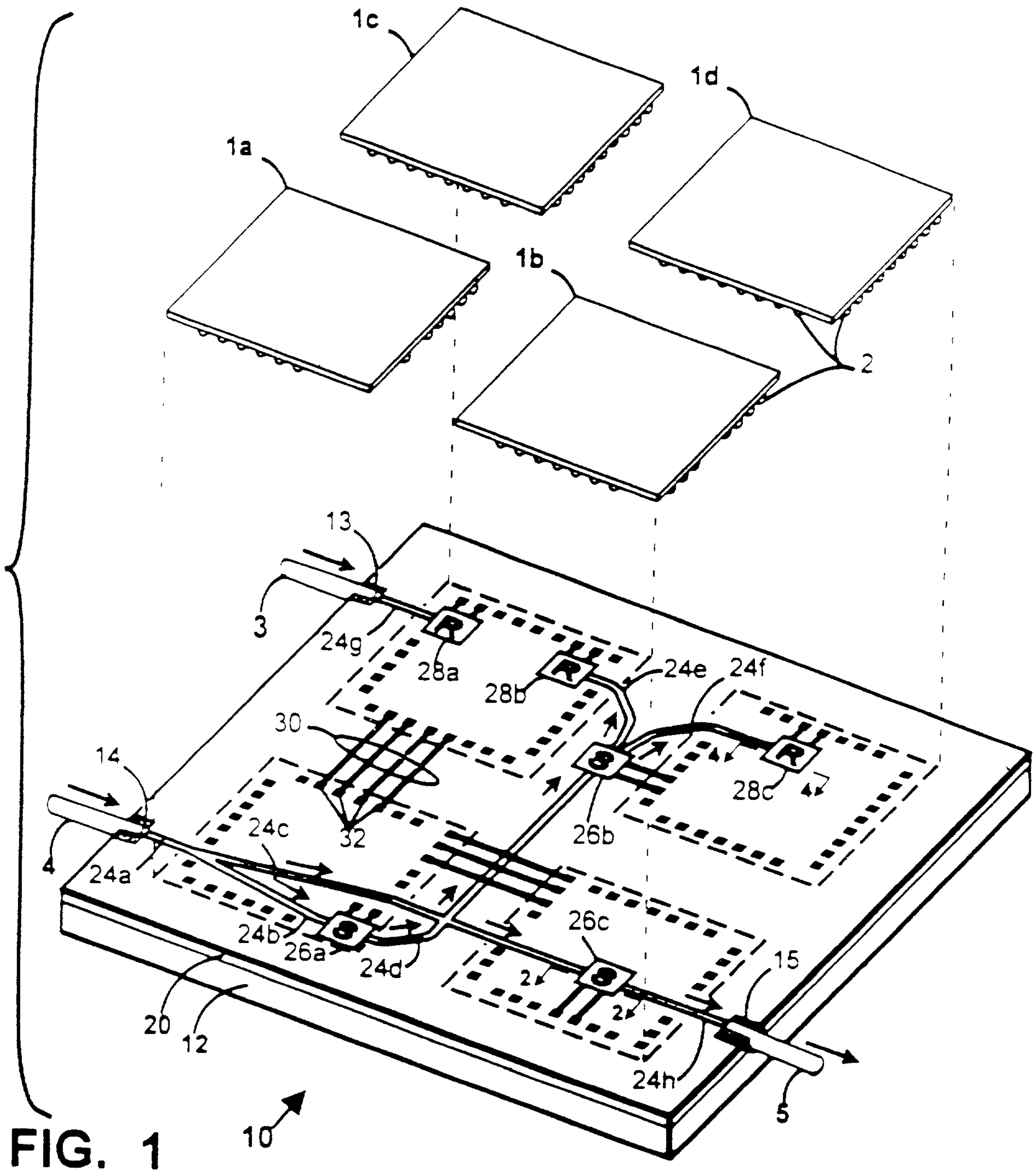


FIG._1

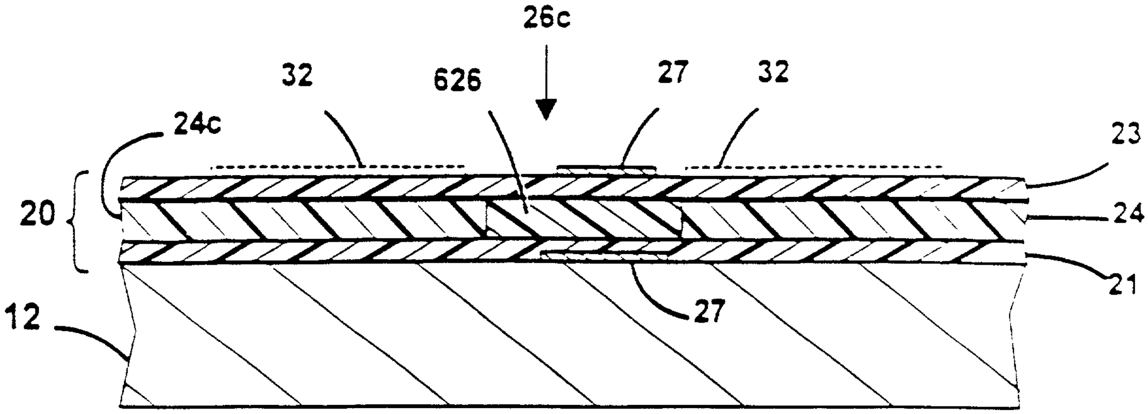

26c
32
626
27
32
24c
23
20
24i
21
12
27

FIG._2

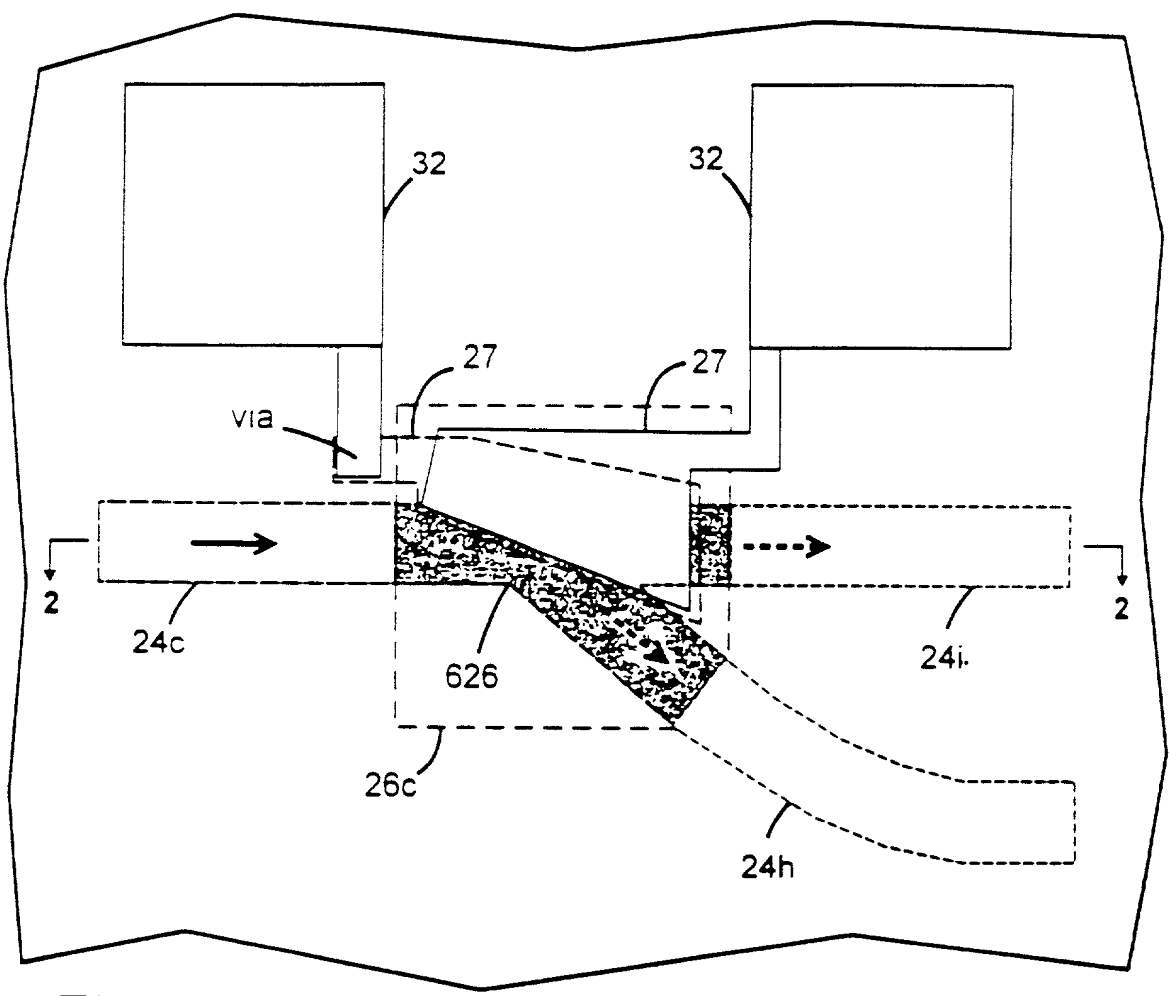

32
32
27
27
via
2
24c
626
26c
24i
2
24h

FIG._3

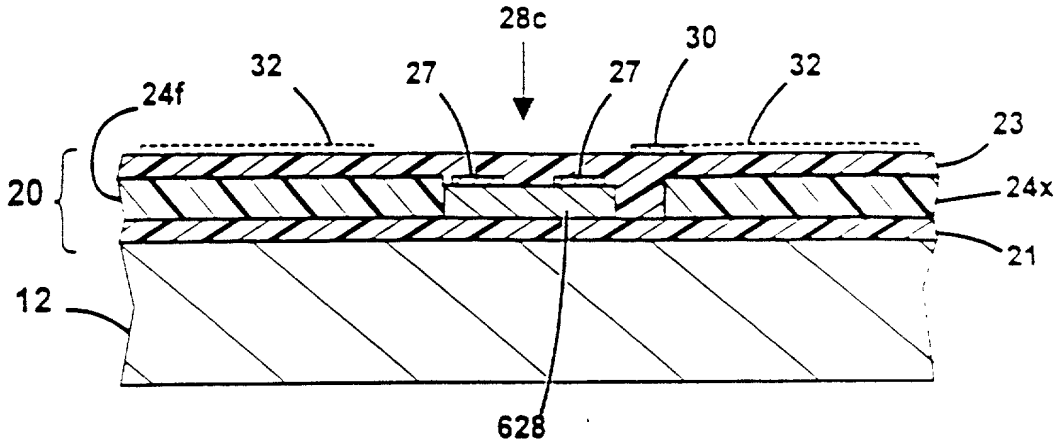

28c
32
27
27
30
32
24f
23
20
24x
21
12
628

FIG._4-1

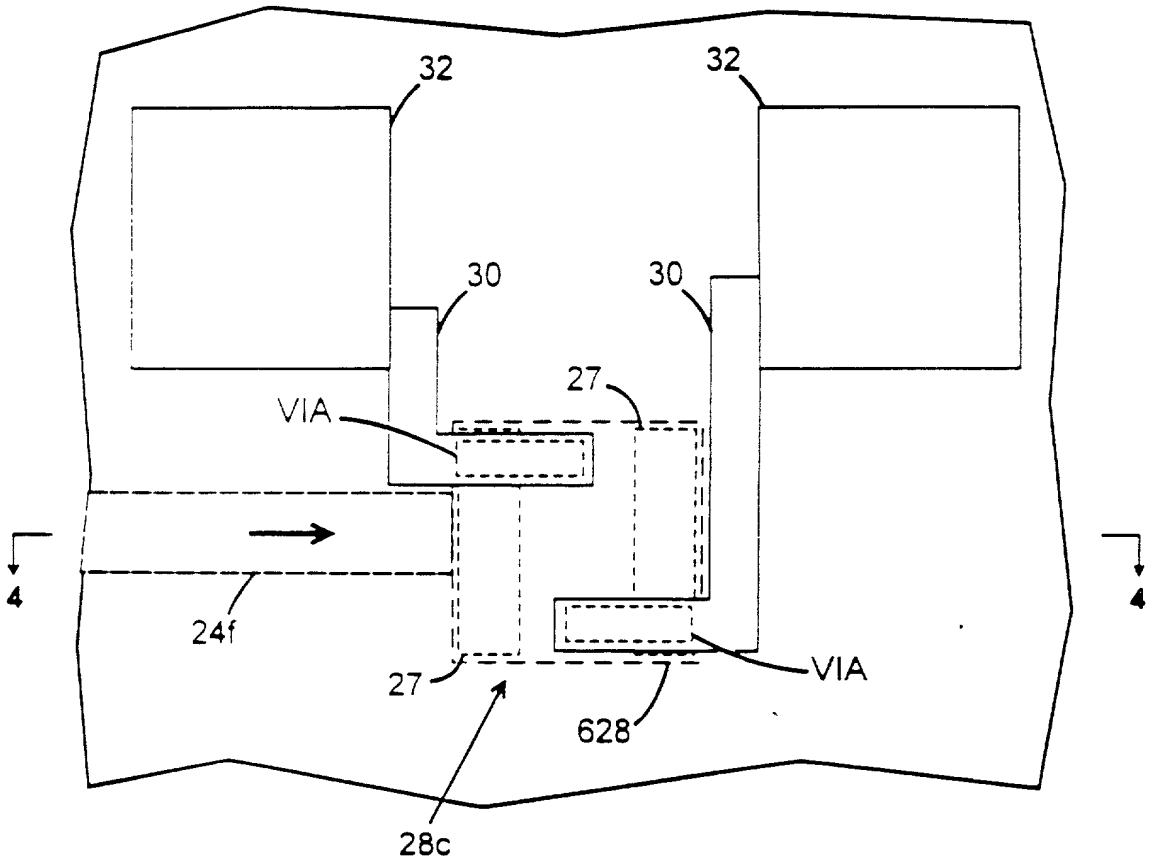

32
32
30
30
27
VIA
4
4
24f
27
VIA
628
28c

FIG._5-1

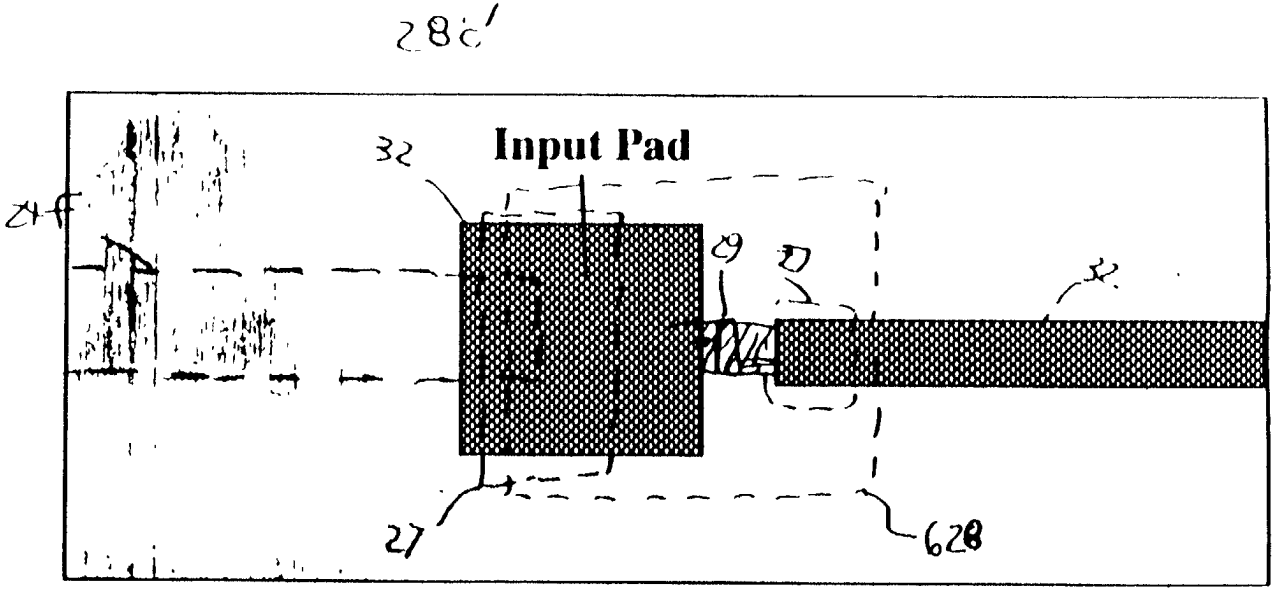


FIG. 5-2

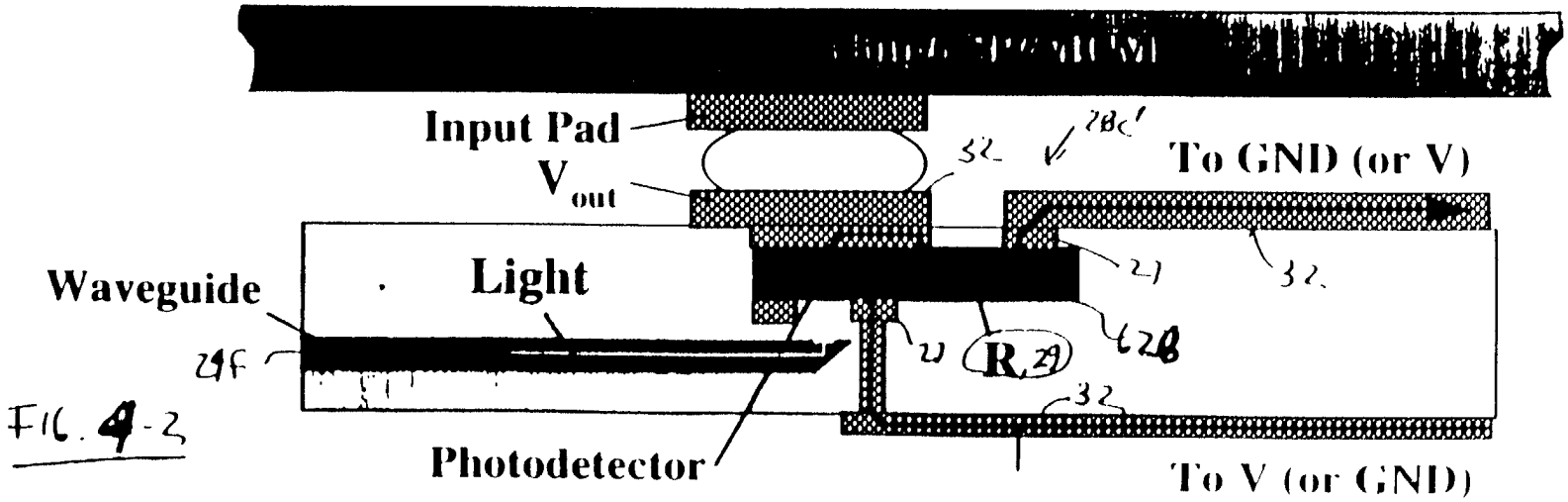


FIG. 4-2

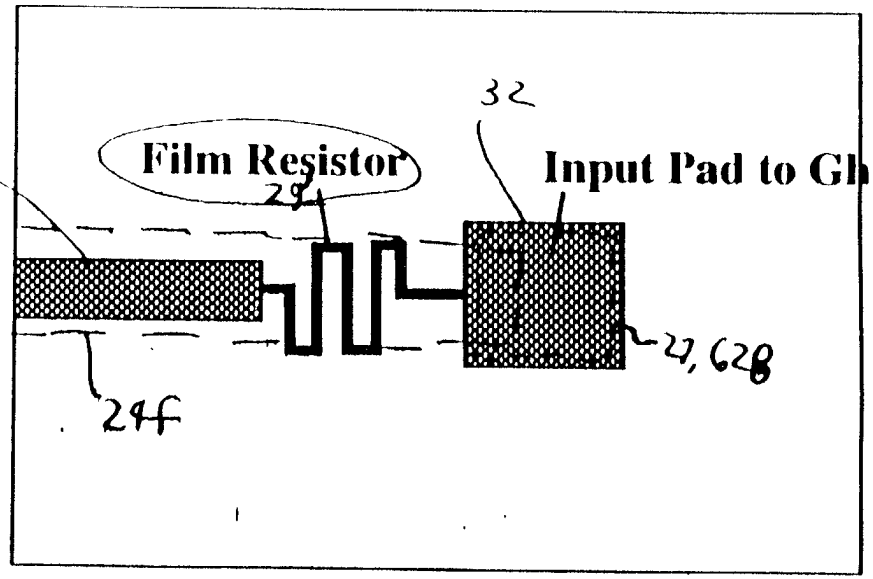


Fig. 5-3

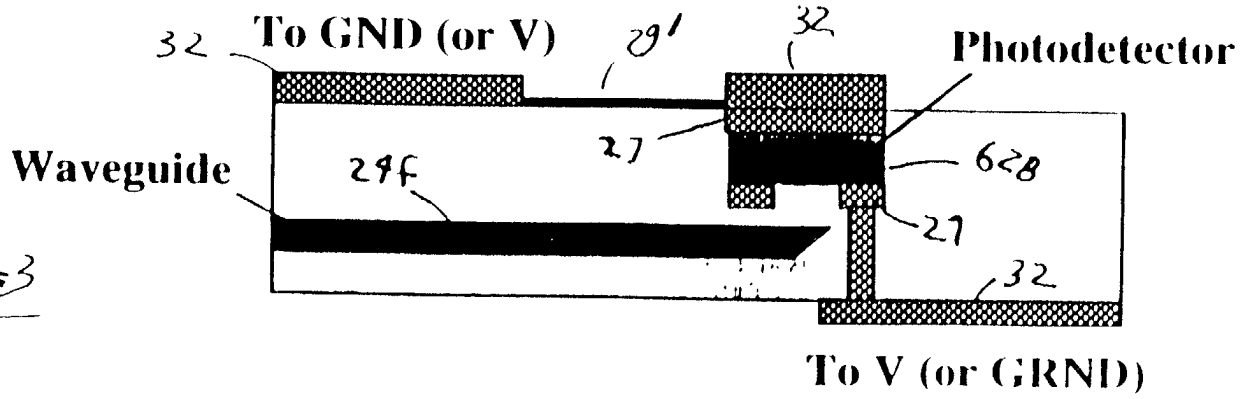


Fig 4-3

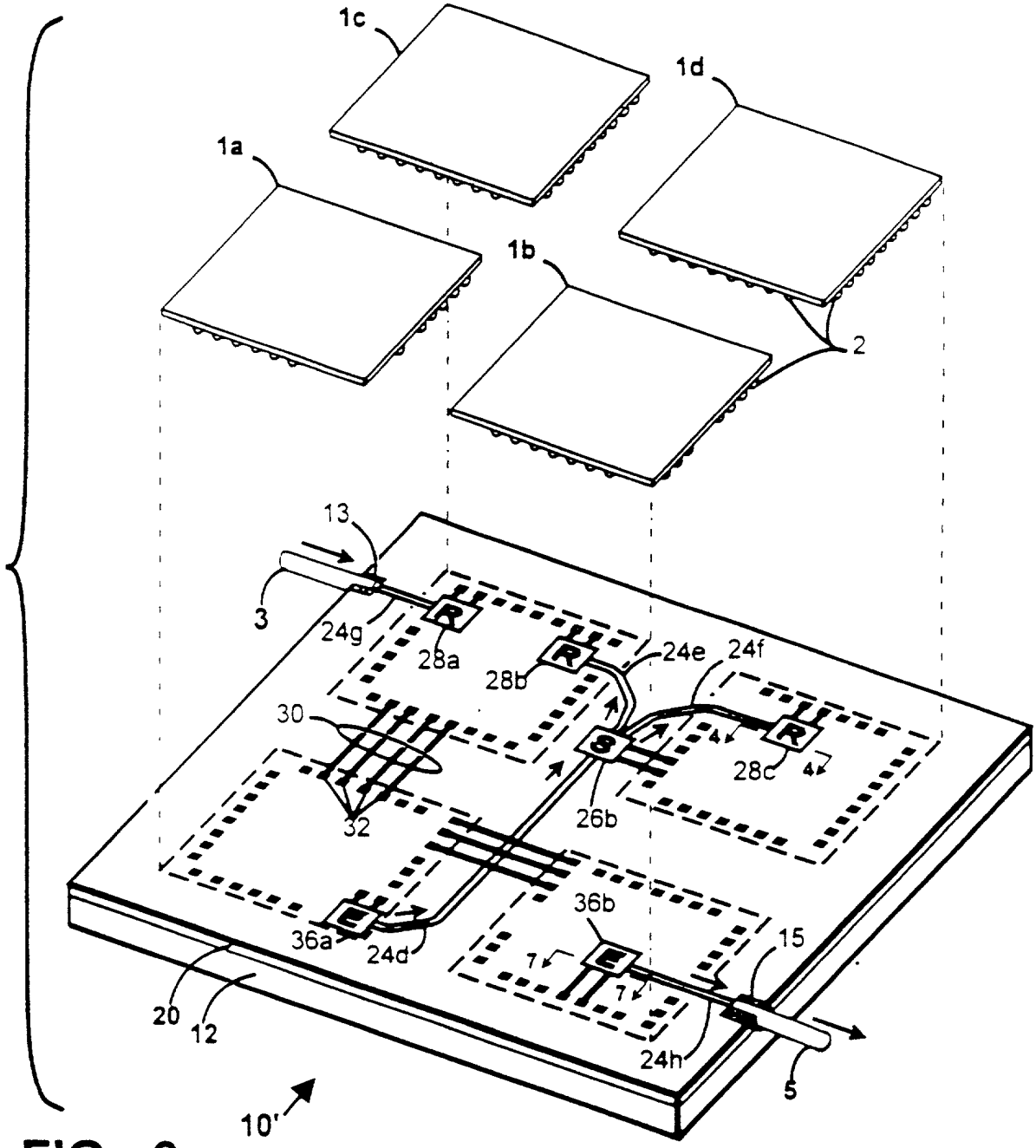

1c
1d
1a
1b
2
13
3
24g
28a
28b
24e
24f
30
32
26b
28c
36b
36a
24d
15
20
12
24h
5
10'

FIG._6

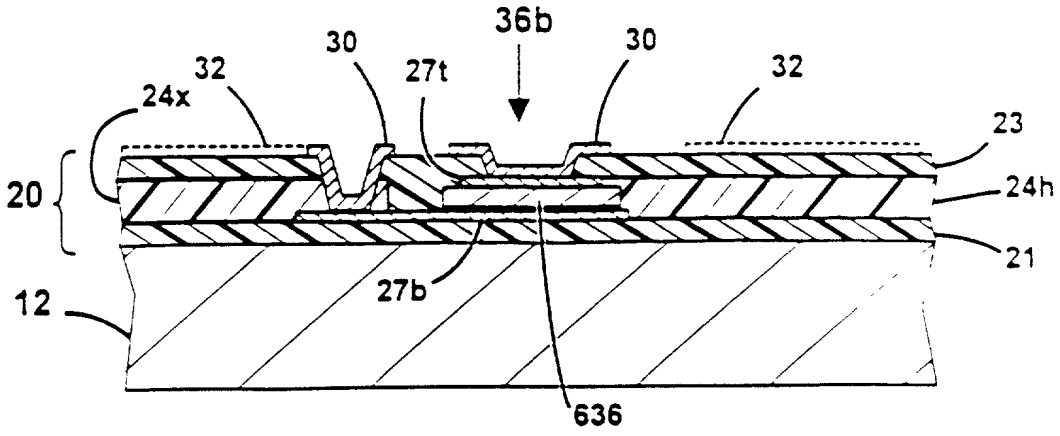

36b
30
30
32
32
27t
24x
23
20
24h
21
12
27b
636

FIG._7

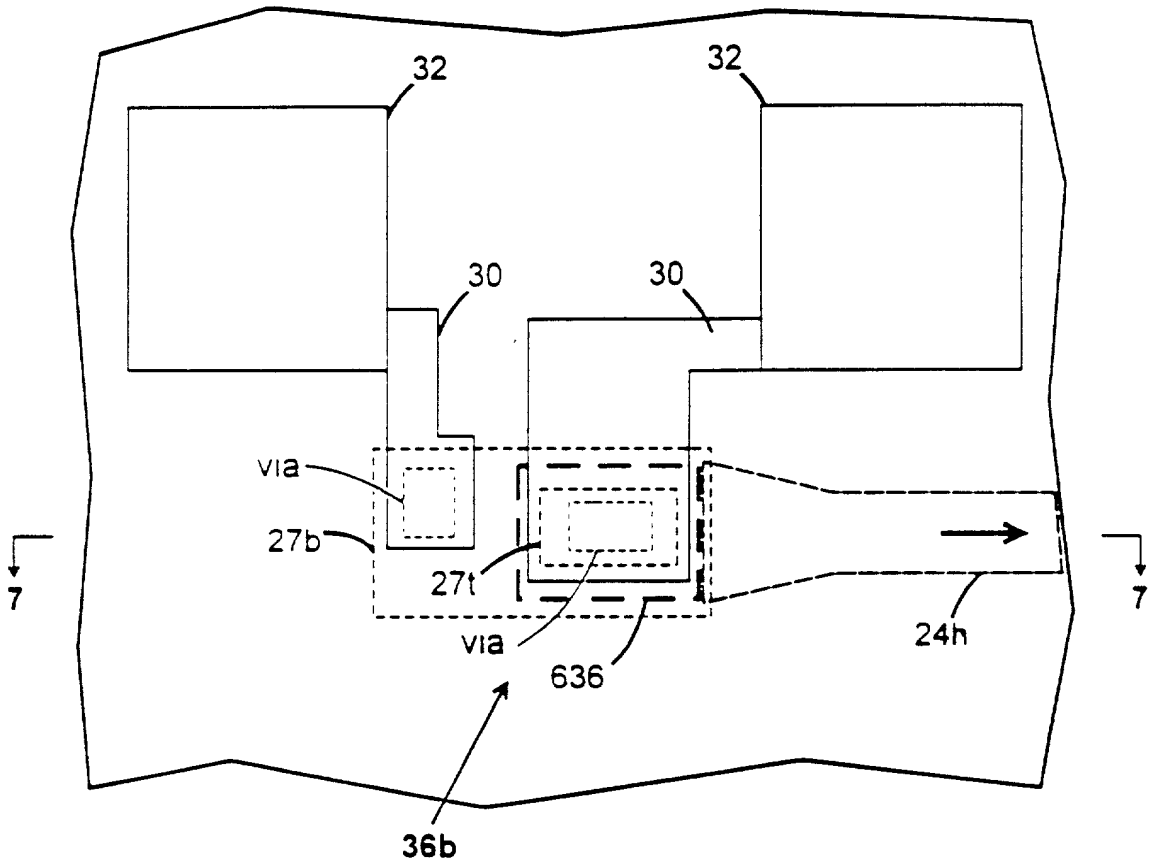

32
32
30
30
via
27b
27t
via
636
24h
7
7
36b

FIG._8

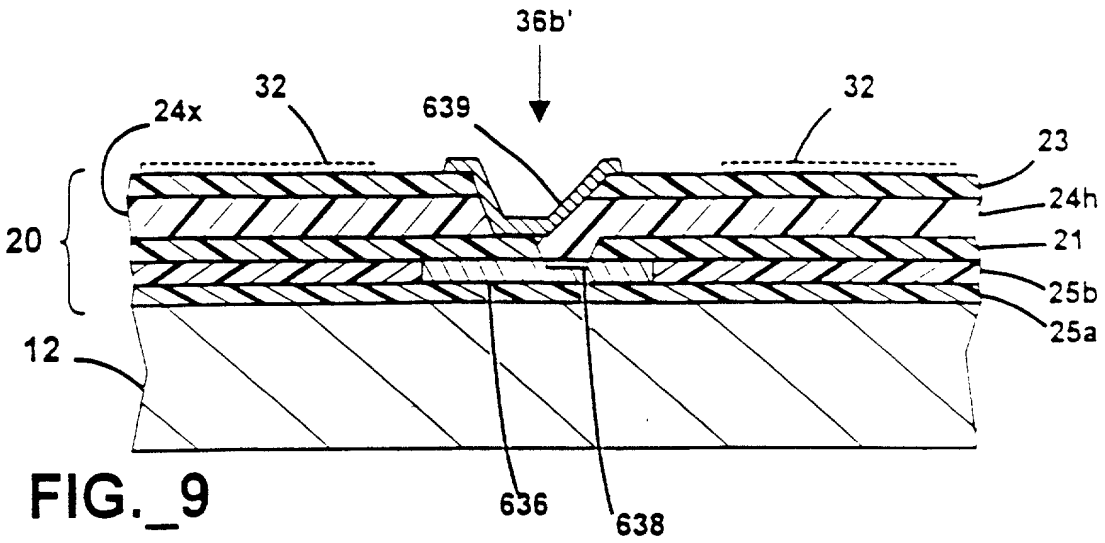

36b'
32
639
32
24x
23
24h
20
21
25b
25a
12
636
638

FIG._9

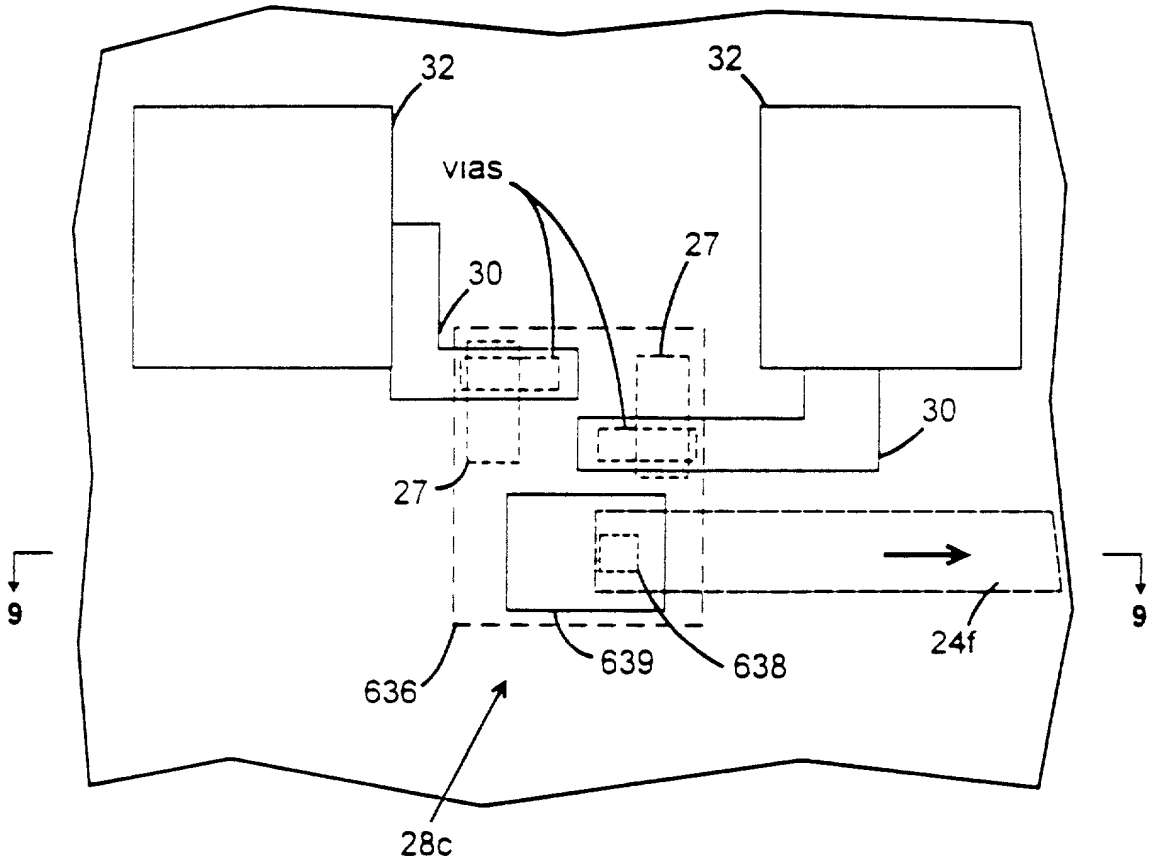

32
32
vias
27
30
30
27
9
9
24f
639
638
636
28c

FIG._10

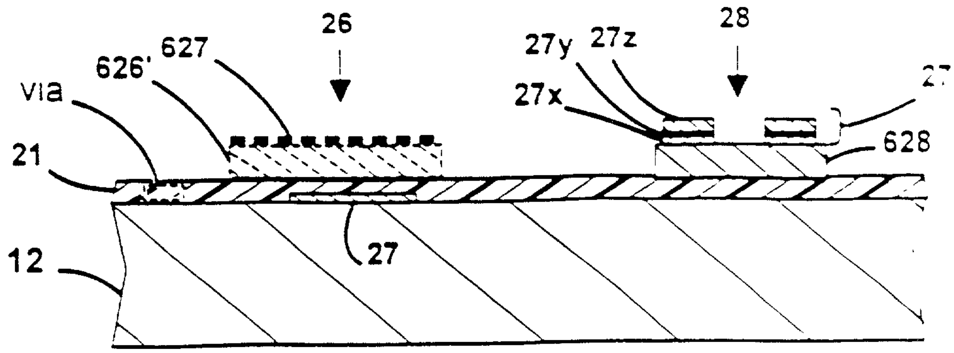


FIG._11

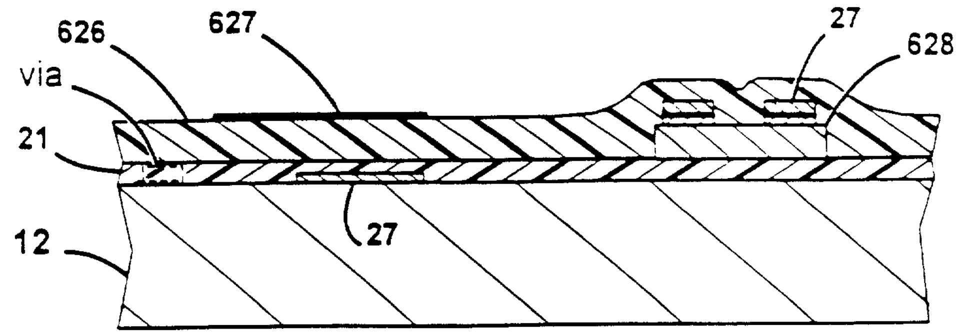


FIG._12

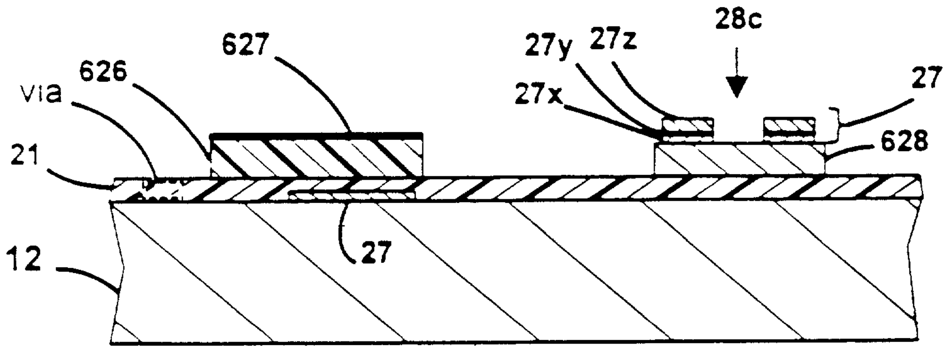


FIG._13

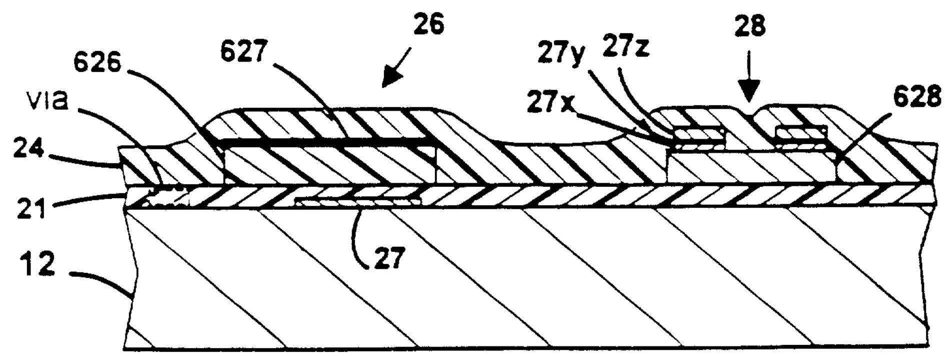


FIG._14

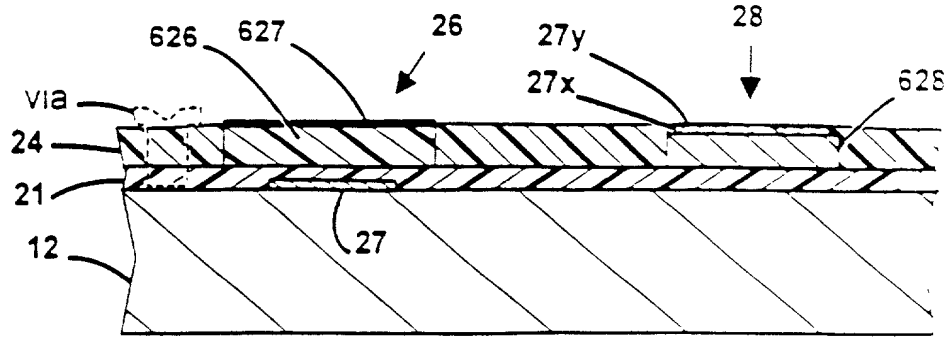


FIG._15

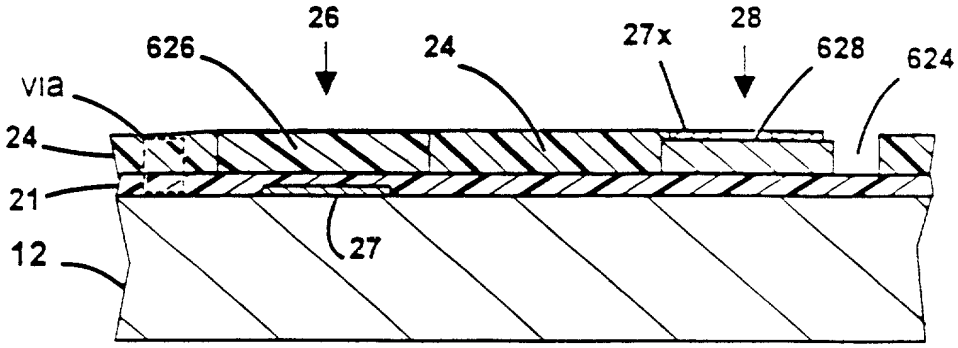


FIG._16

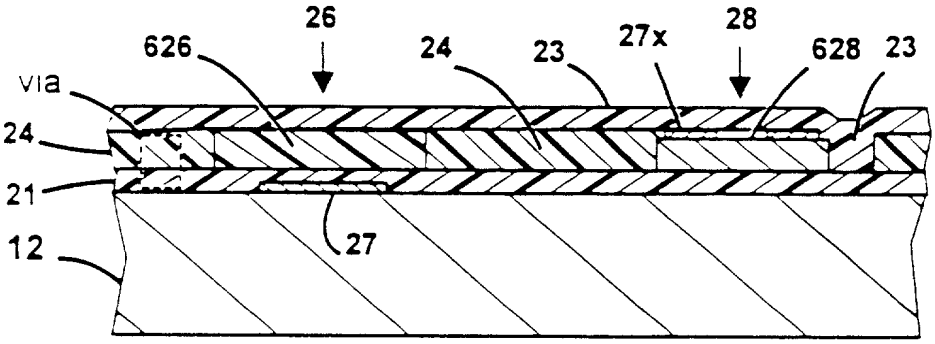


FIG._17

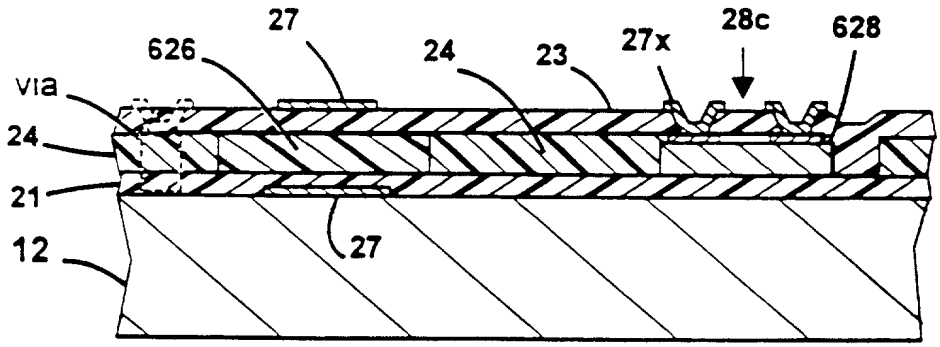


FIG._18

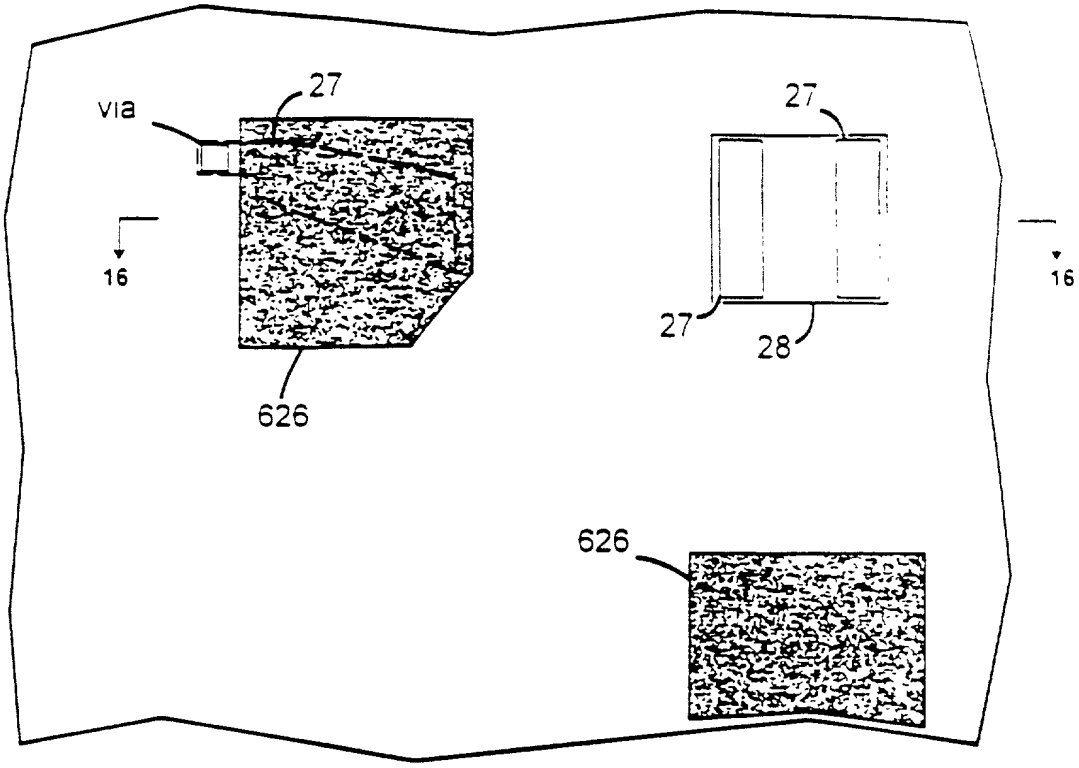

via
27
16
626
27
27
28
16
626

FIG._19

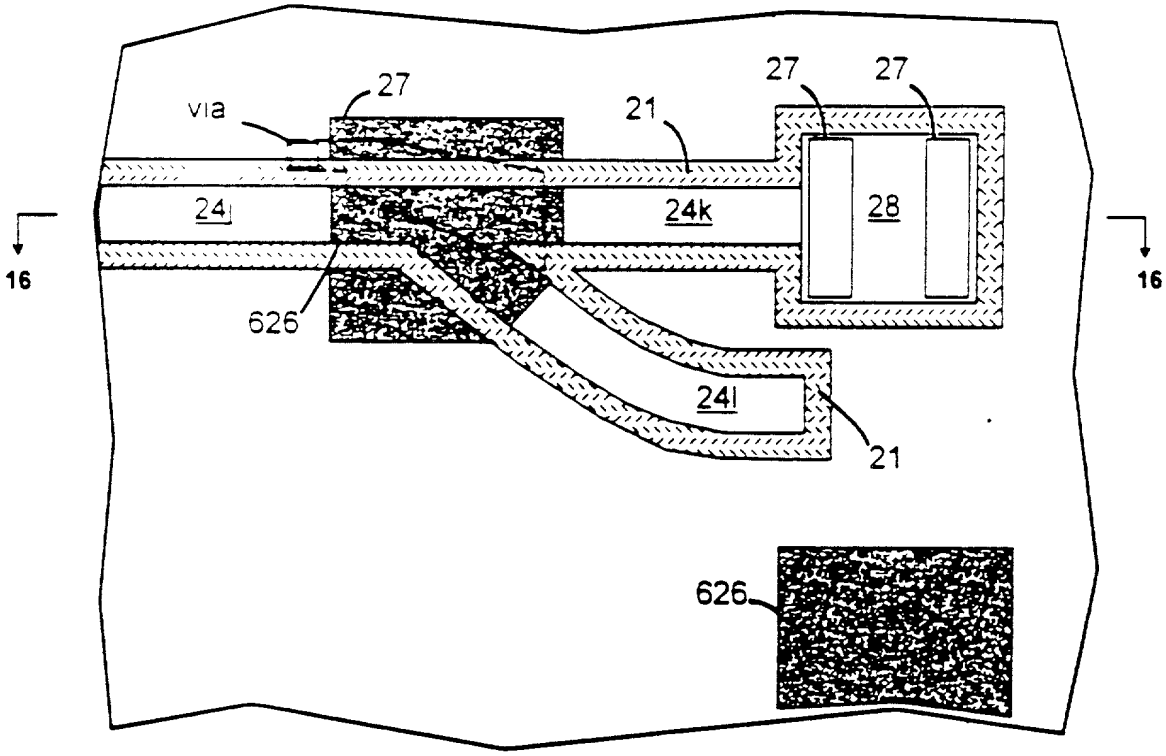

via
27
21
27
27
24j
24k
28
16
626
24l
21
16
626

FIG._20

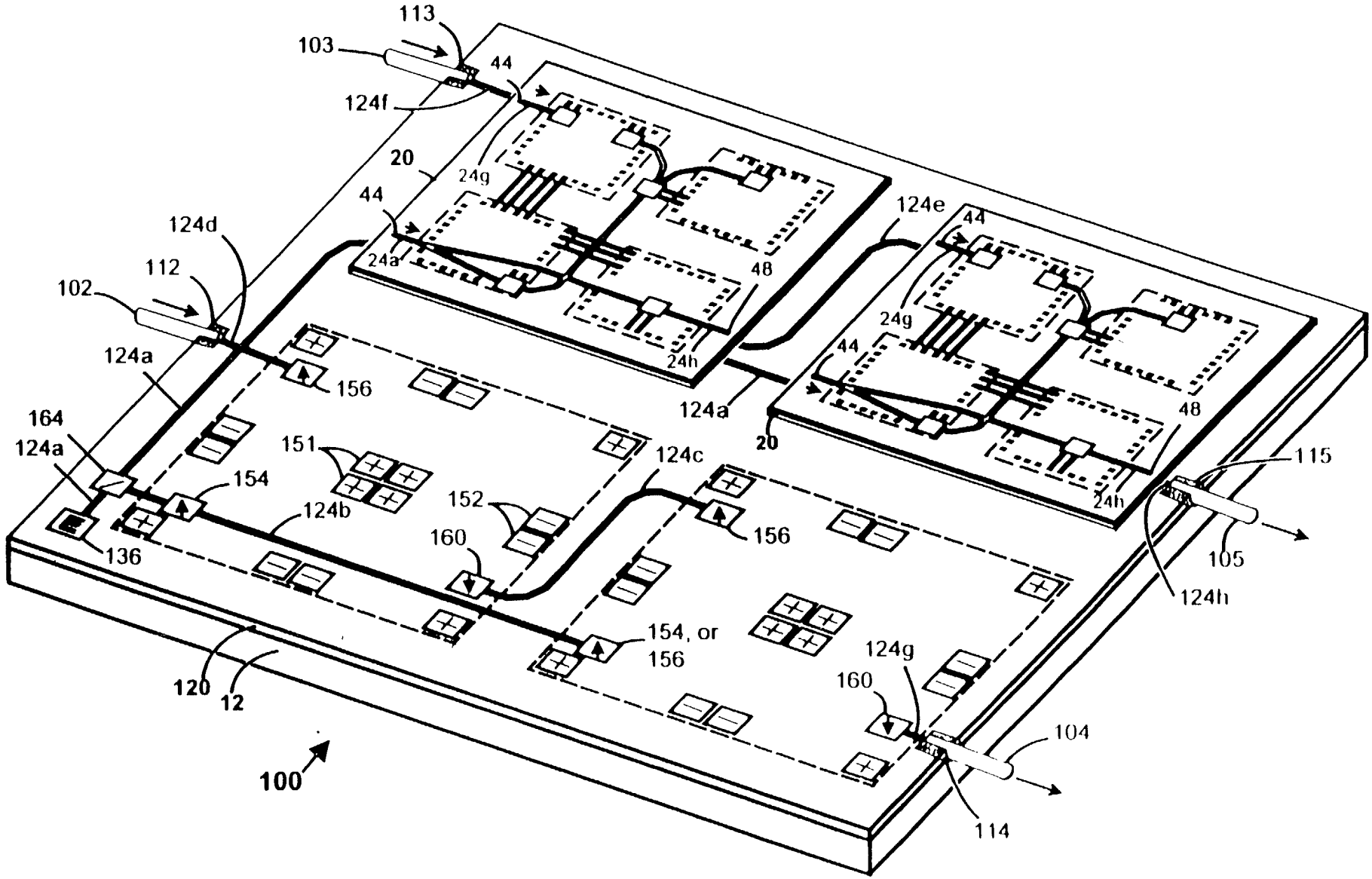

113
103
44
124f
20
24g
44
124d
112
102
24a
48
124e
44
24g
124a
156
44
48
164
124a
151
124c
115
154
152
124b
160
156
136
105
124h
154, or
156
124g
160
120
12
104
100
114

FIG. 21

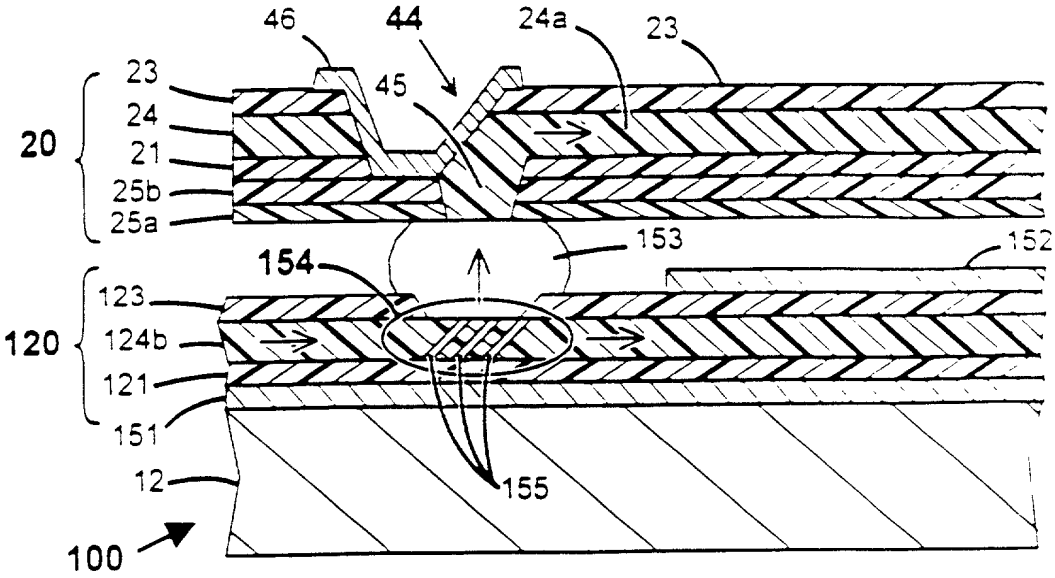

46
44
24a
23
23
24
21
25b
25a
20
45
153
152
154
123
124b
121
120
151
12
155
100

FIG._22

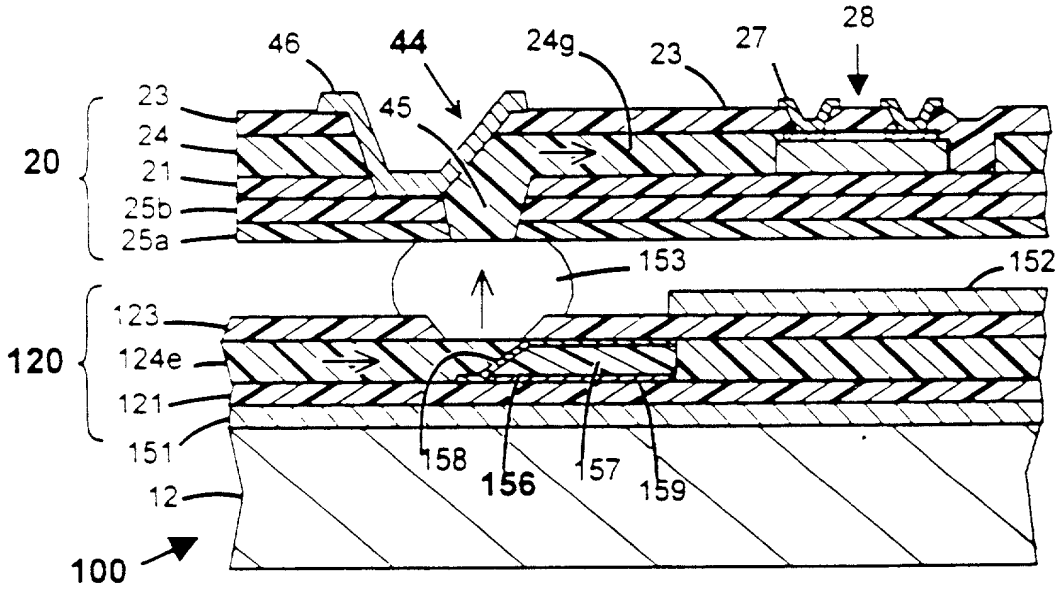

46
44
24g
23
27
28
23
24
21
25b
25a
20
45
153
152
123
124e
121
120
151
158
156
157
159
12
100

FIG._23

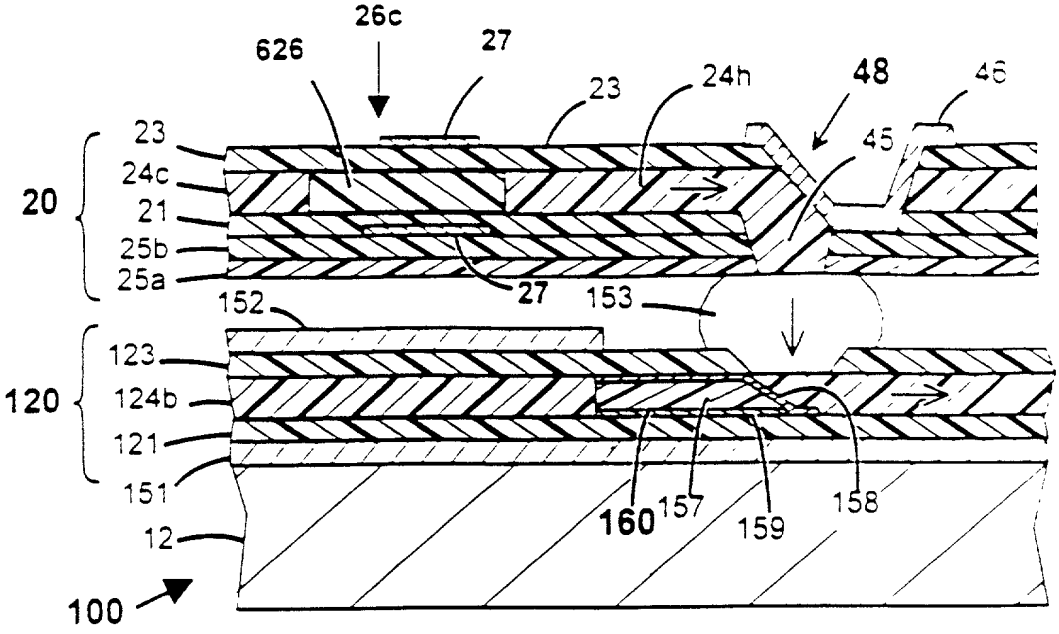


FIG._24

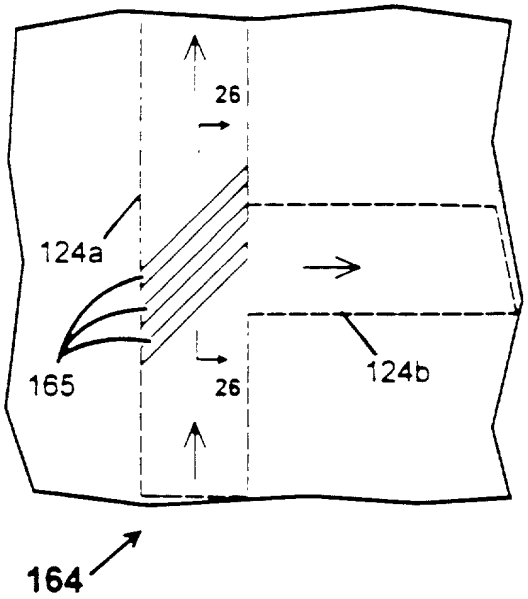


FIG._25

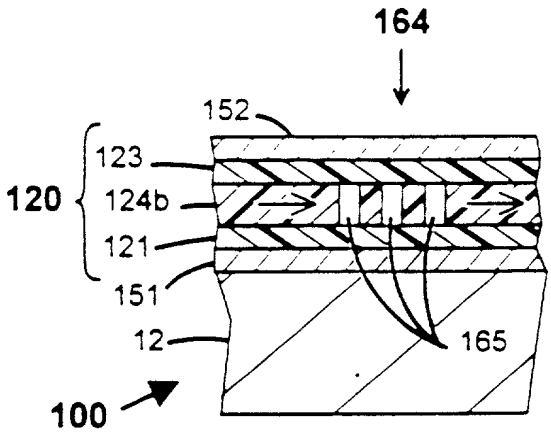


FIG._26

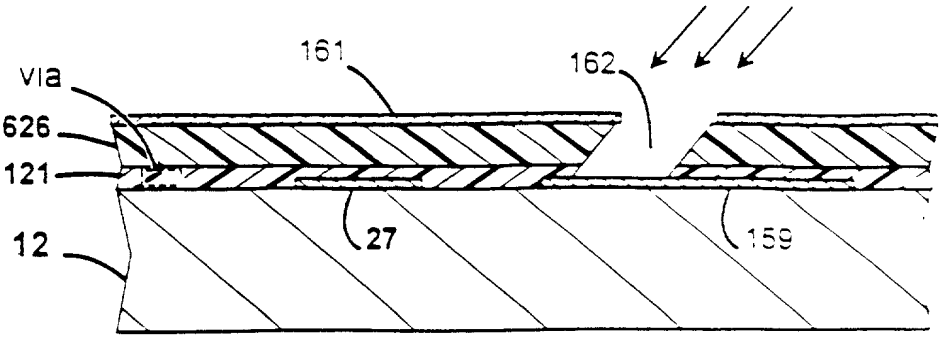


FIG._27

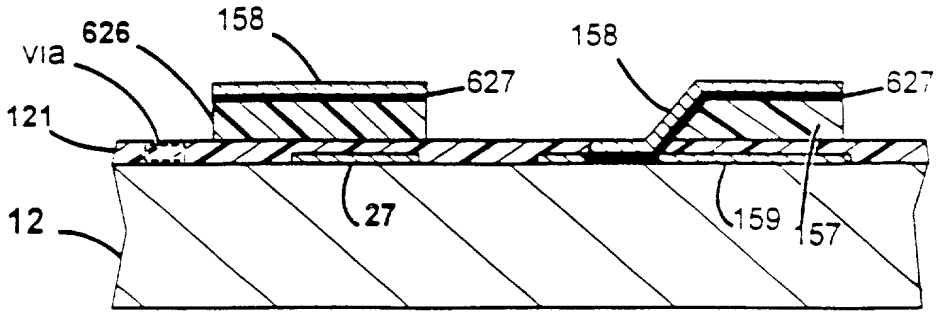


FIG._28

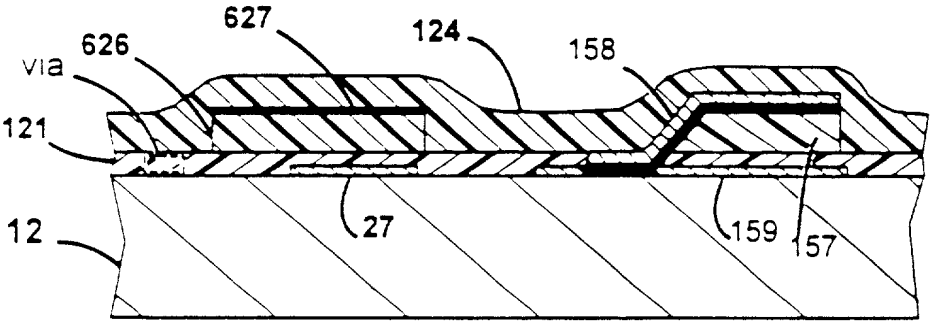


FIG._29

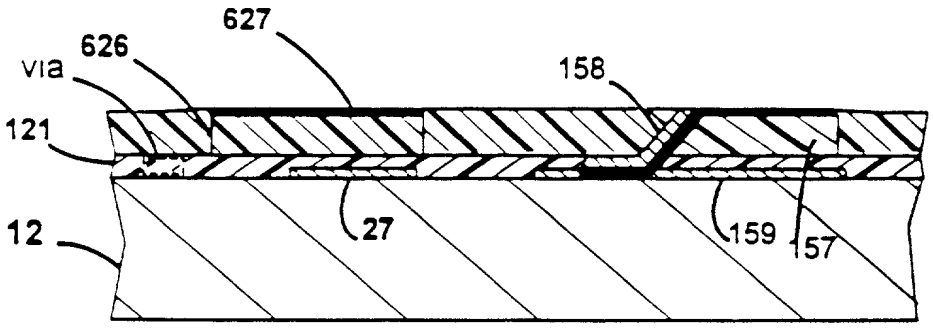


FIG._30

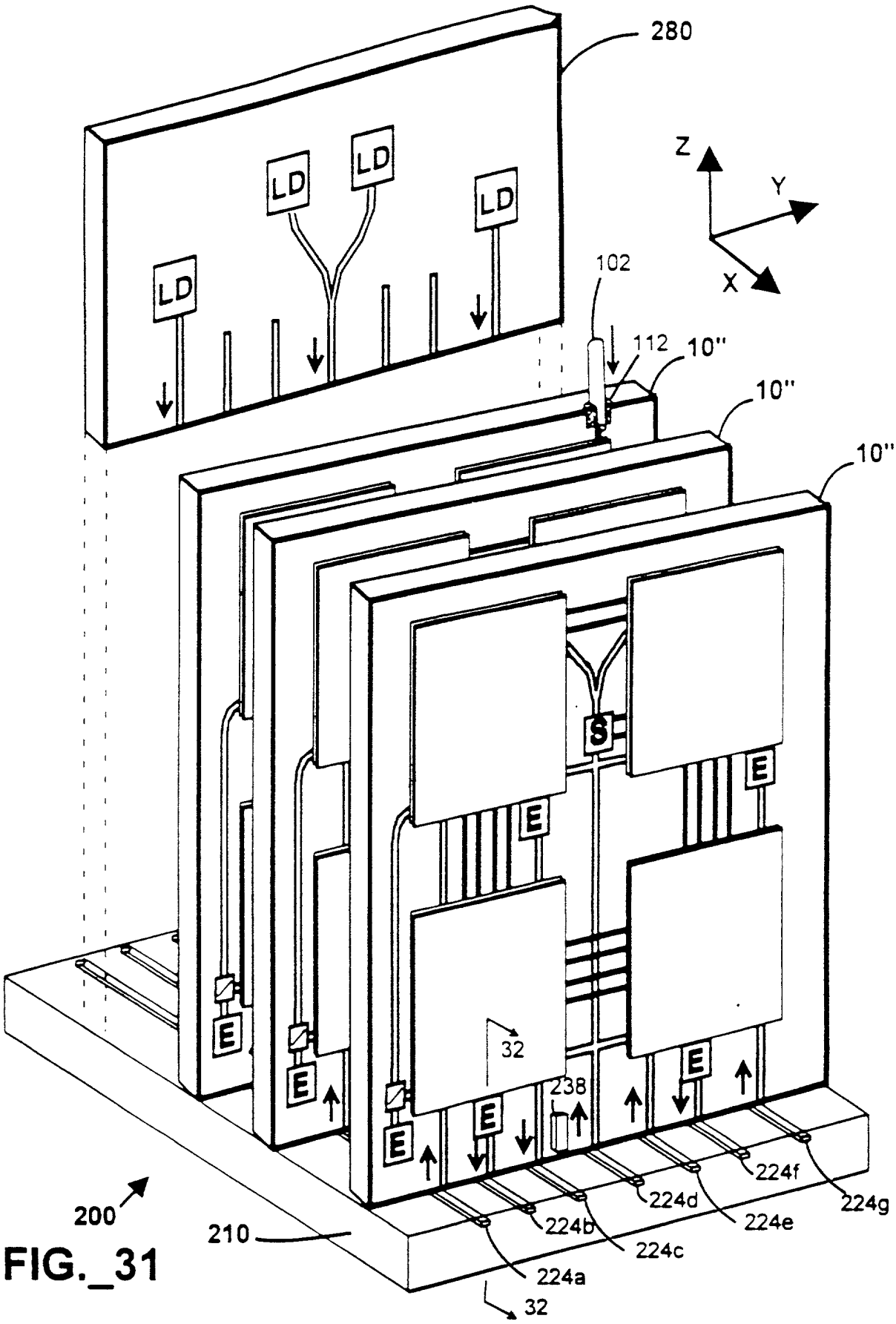

280
LD
LD
LD
LD
Z
Y
X
102
112
10''
10''
10''
S
E
E
E
E
E
E
E
E
32
238
224f
224d
224e
224g
224b
224c
224a
32
200
210

FIG._31

FIG._32

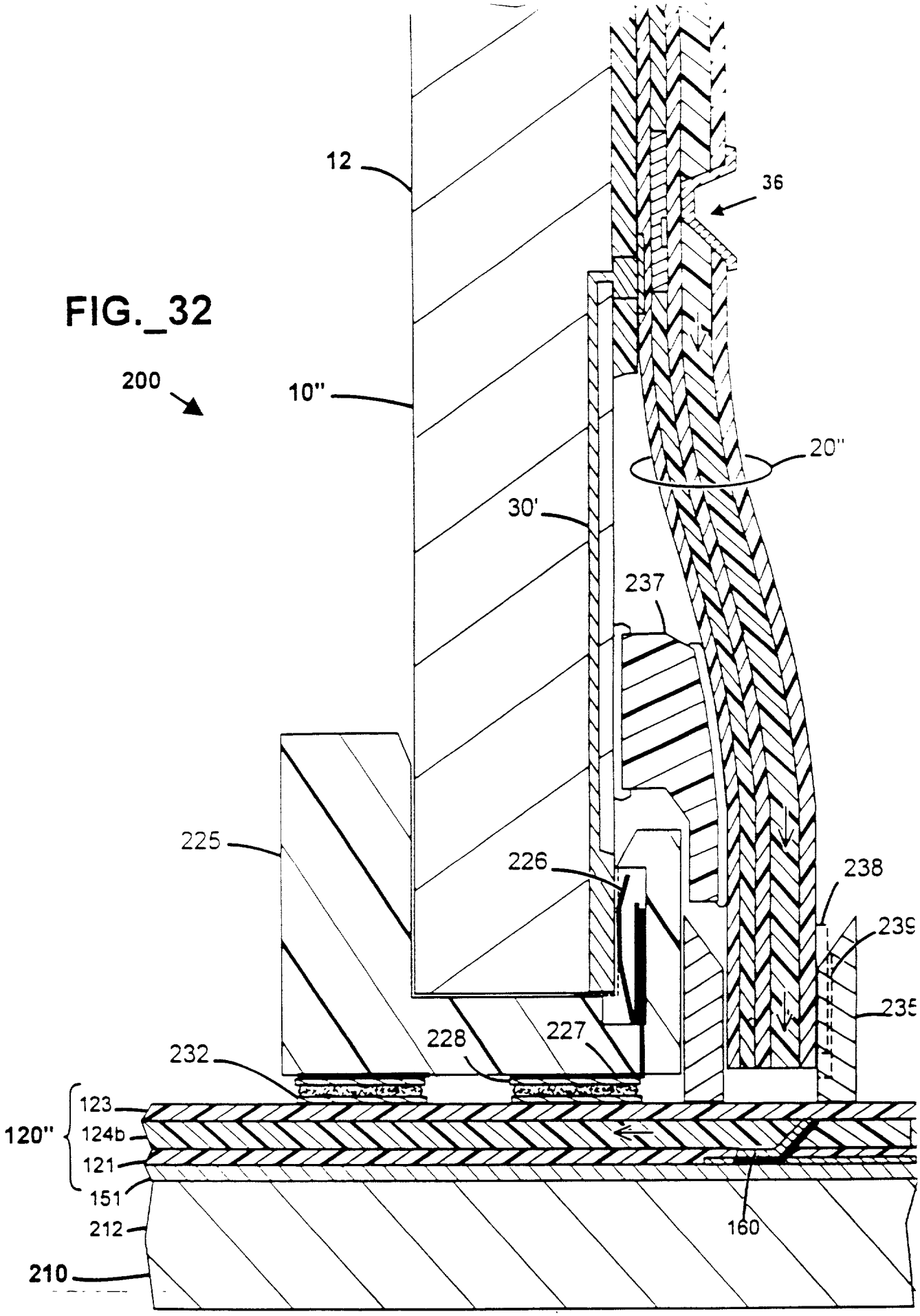
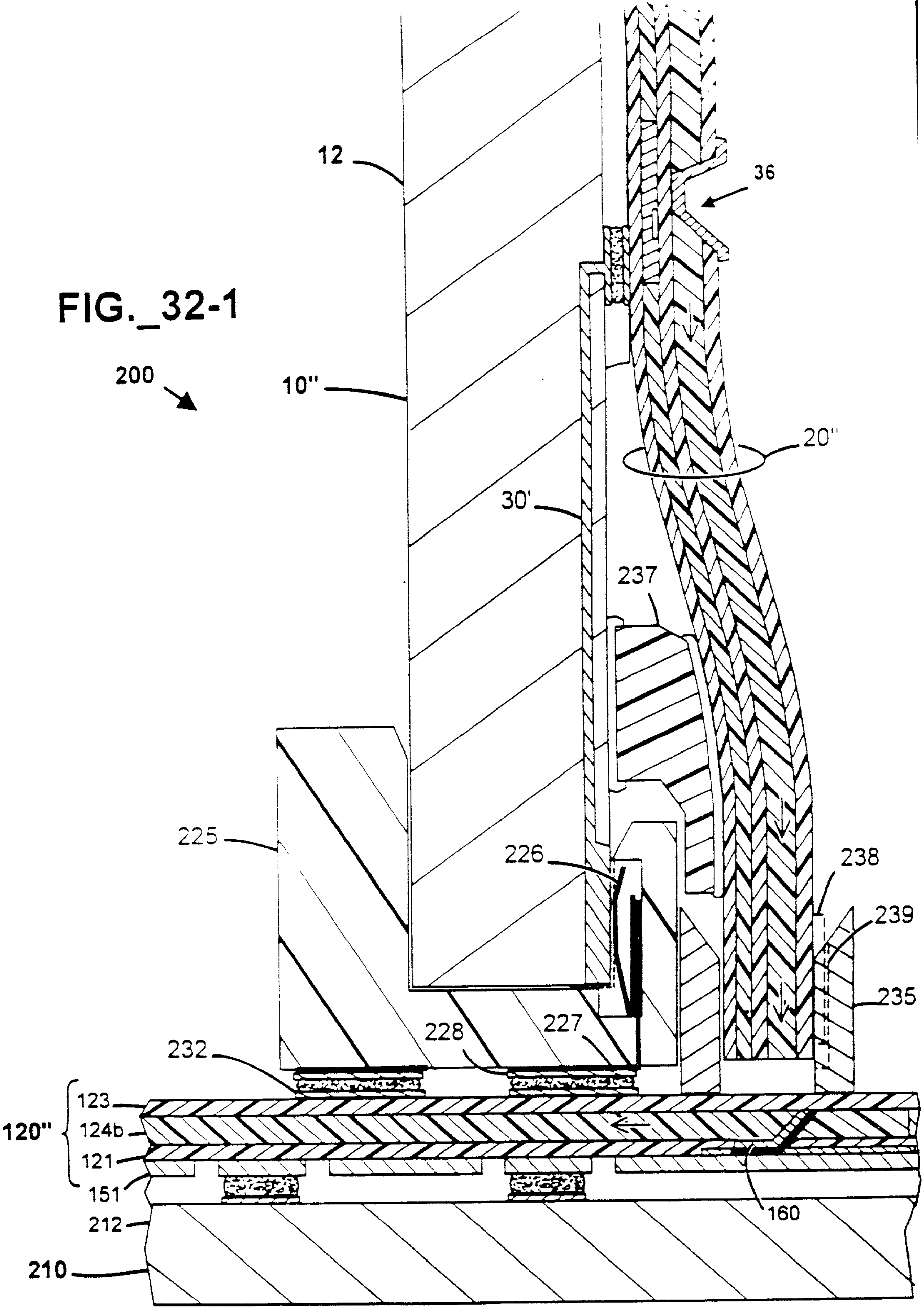

200
12
36
10"
20"
30'
237
225
226
238
239
235
228
227
232
123
120"
124b
121
151
212
210
160

FIG._32-1



12
36
200
10"
20"
30'
237
225
226
238
239
235
232
228
227
123
120"
124b
121
151
160
212
210

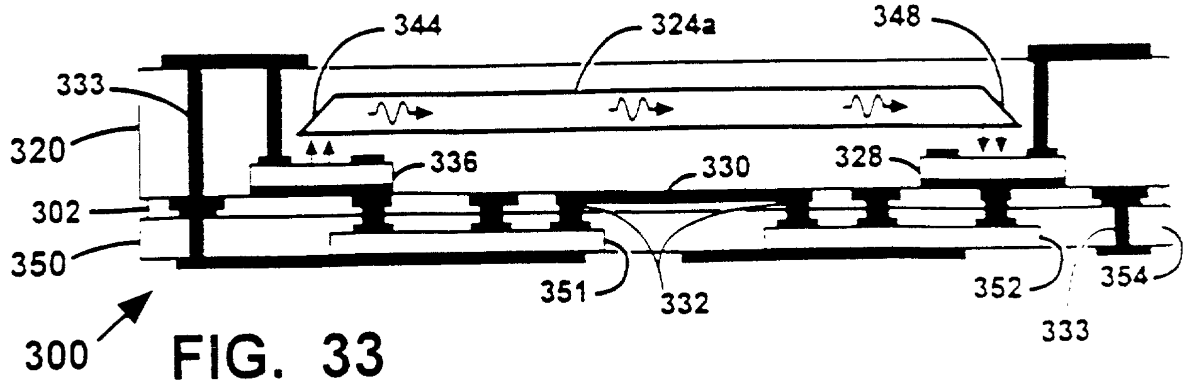


FIG._33

FIG._34

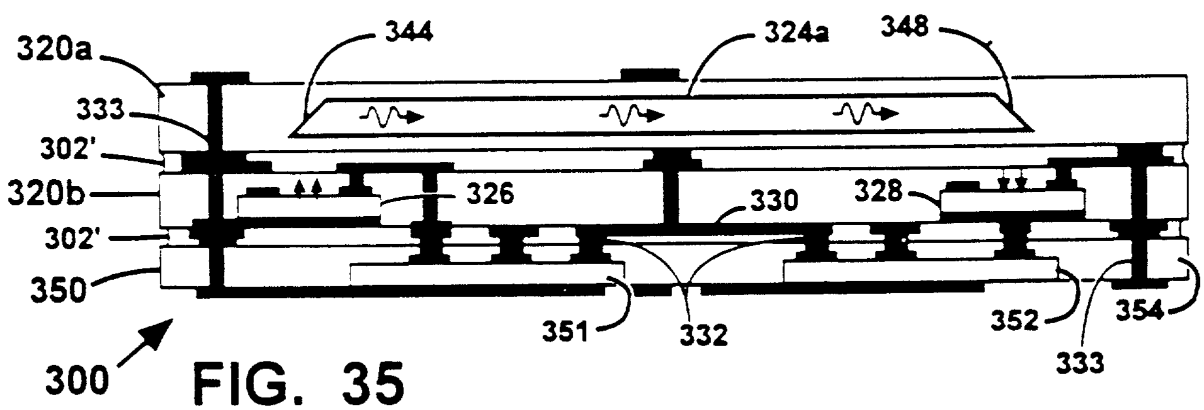


FIG._35

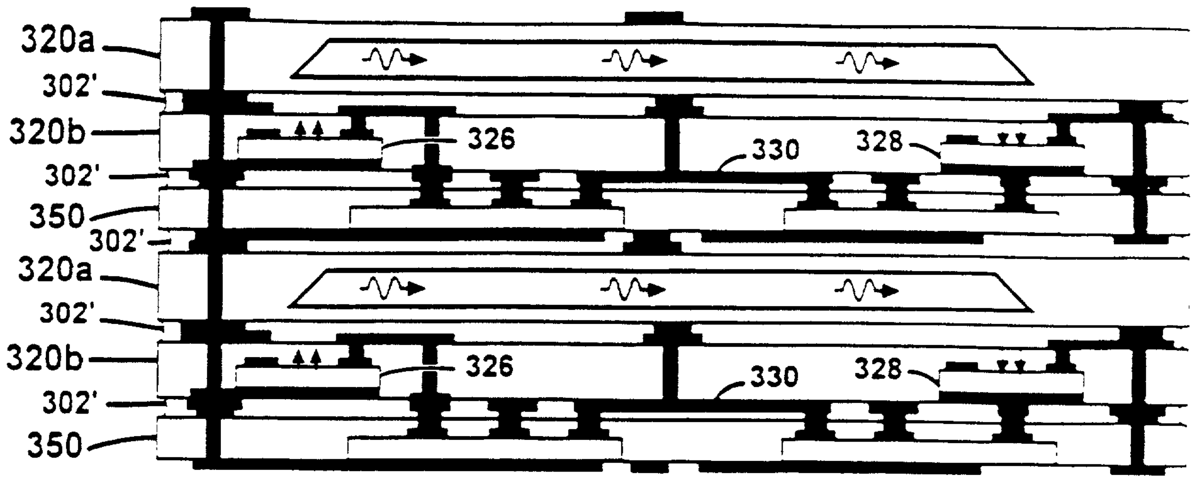


FIG._36

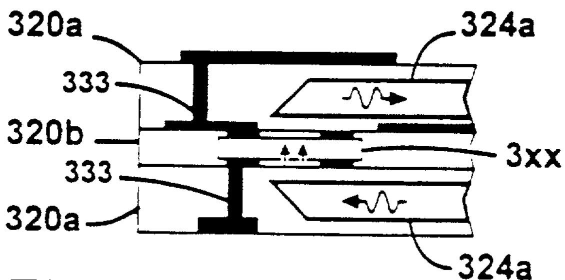


FIG._37-1

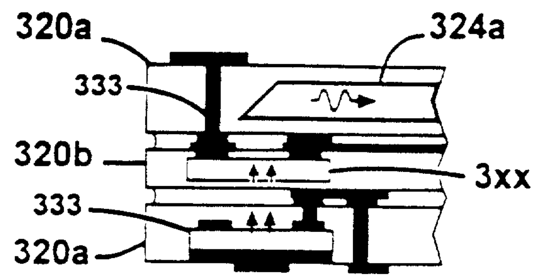


FIG._37-2

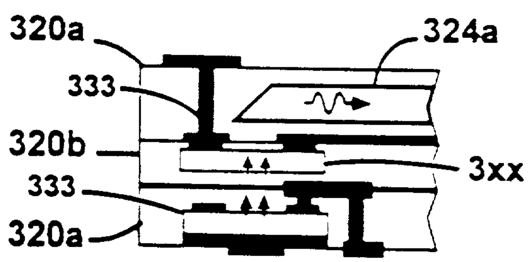


FIG._37-3

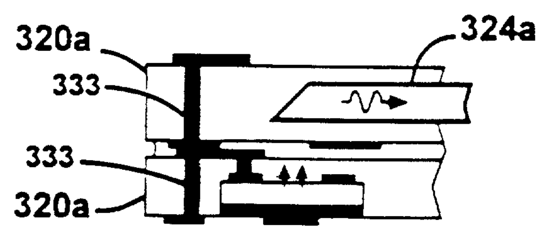


FIG._37-4

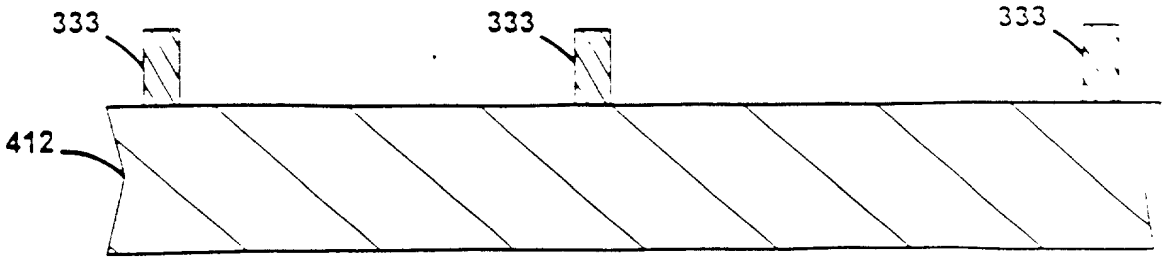


FIG._38

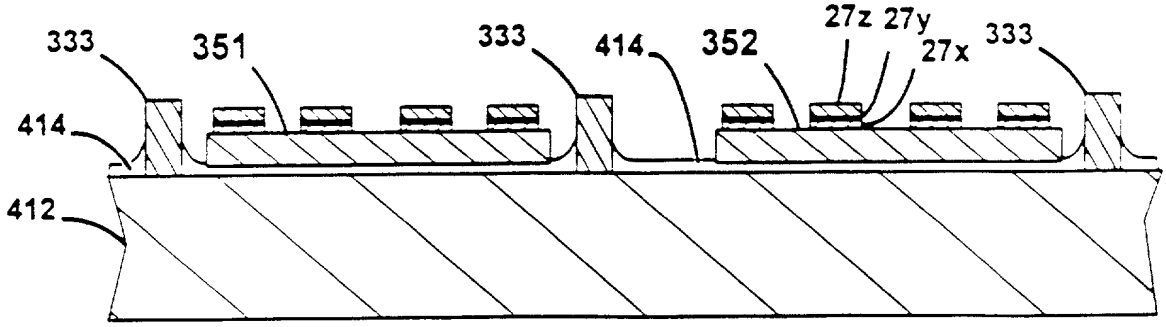


FIG._39

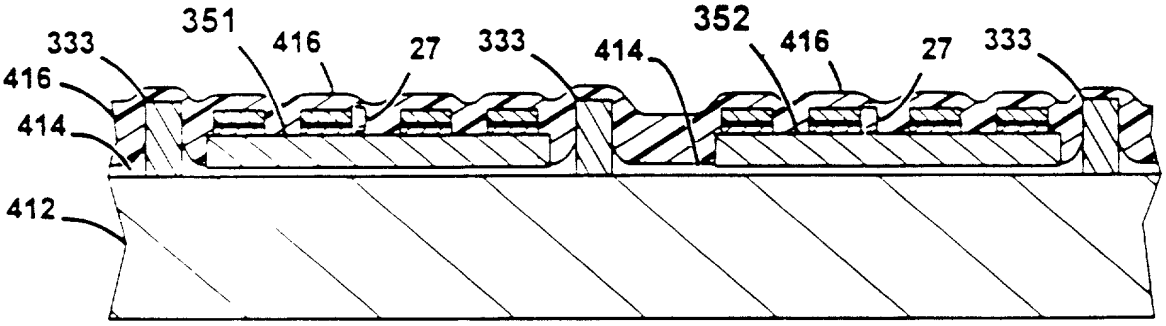


FIG._40

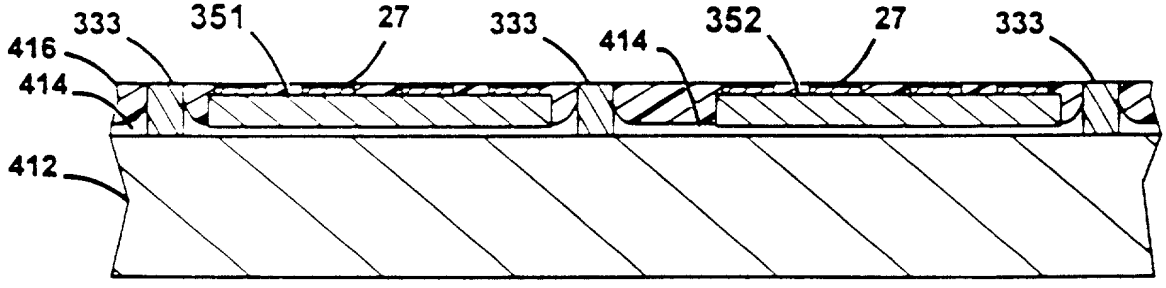


FIG._41

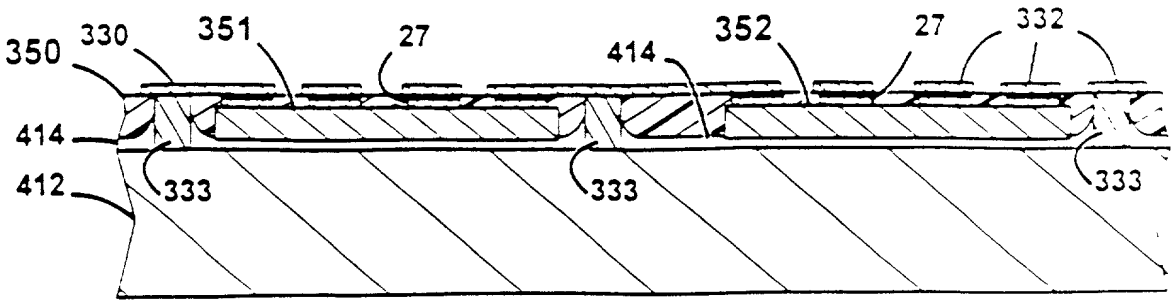


FIG._42

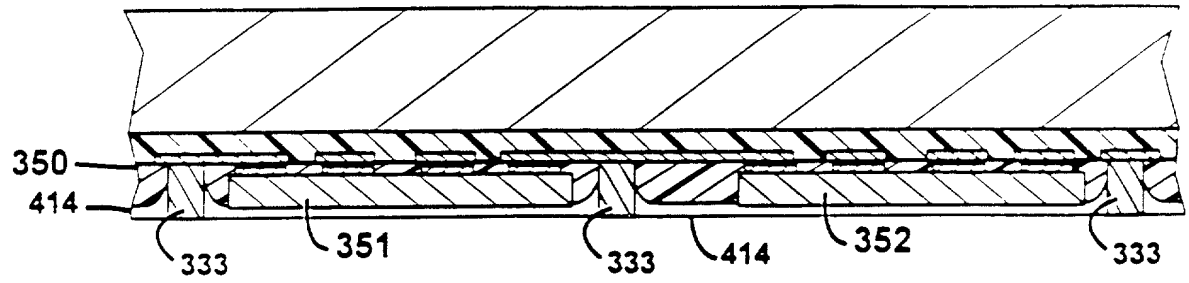


FIG._43

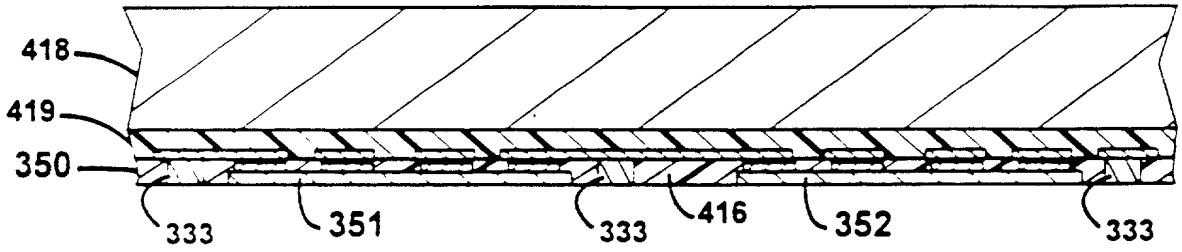


FIG._44

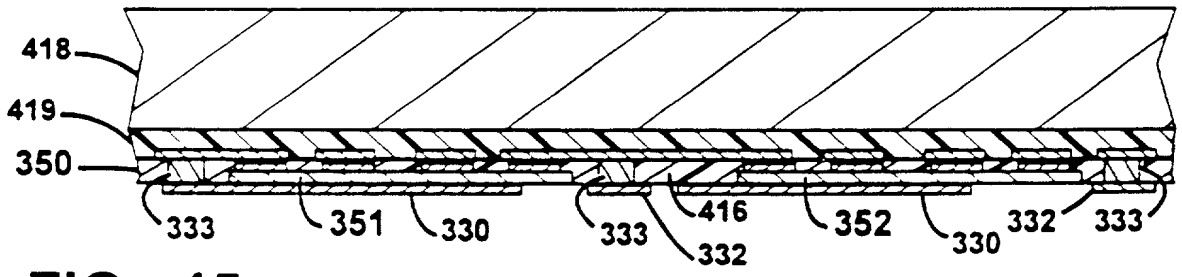


FIG._45

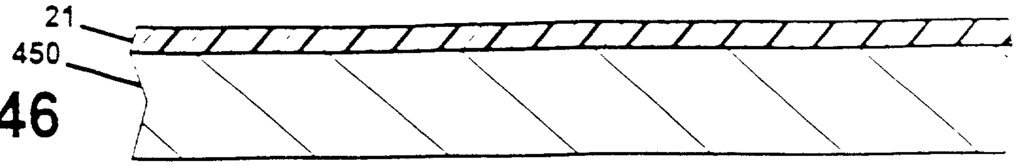


FIG._46

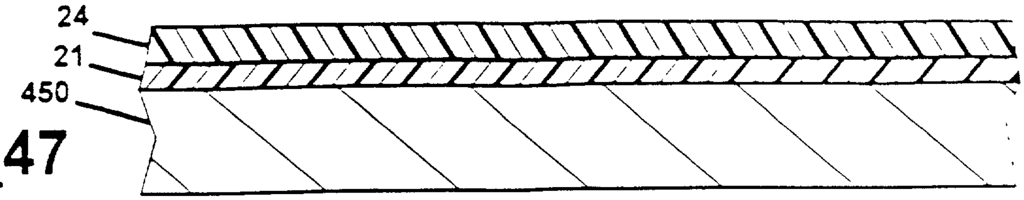


FIG._47

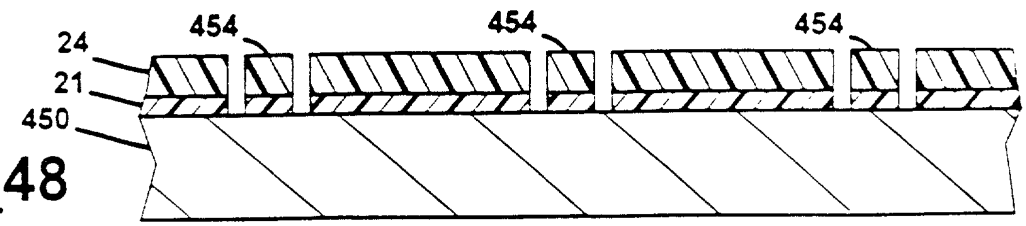


FIG._48

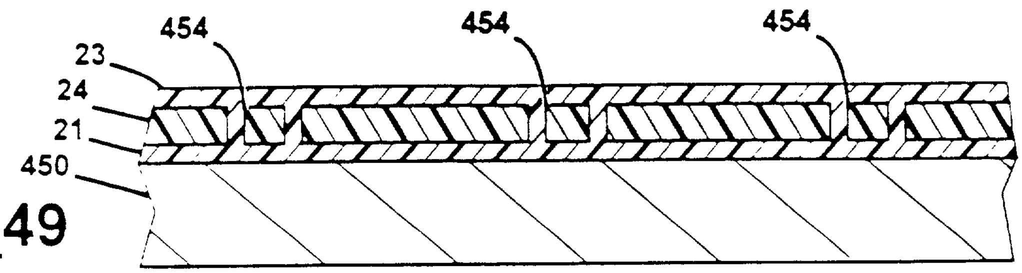


FIG._49

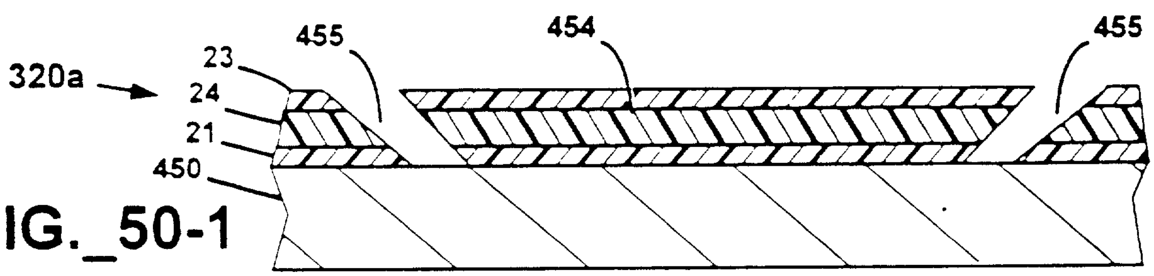


FIG._50-1

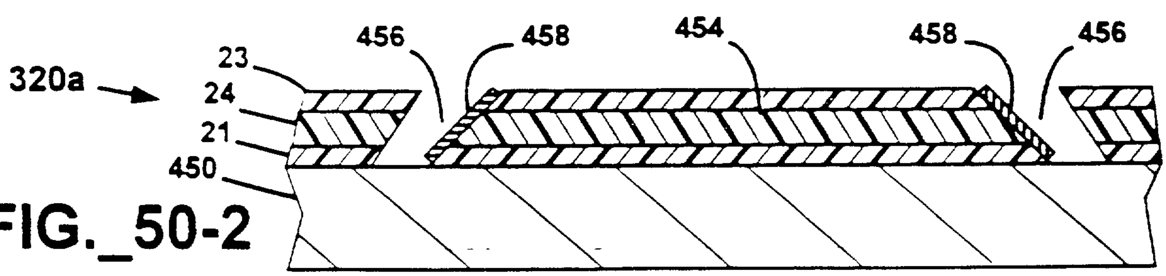


FIG._50-2

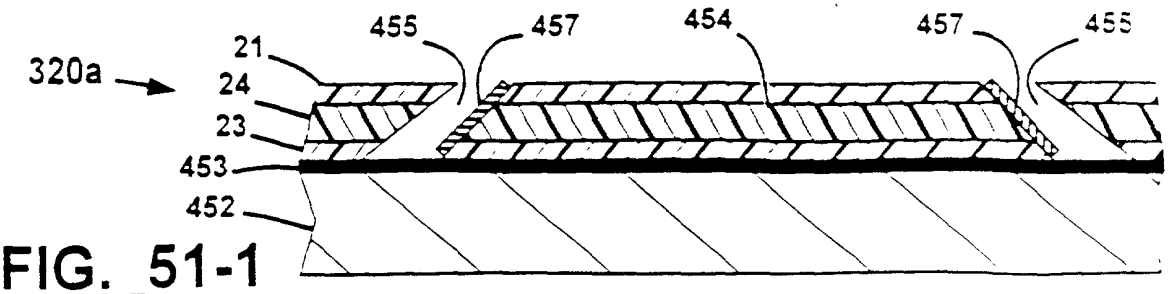


FIG._51-1

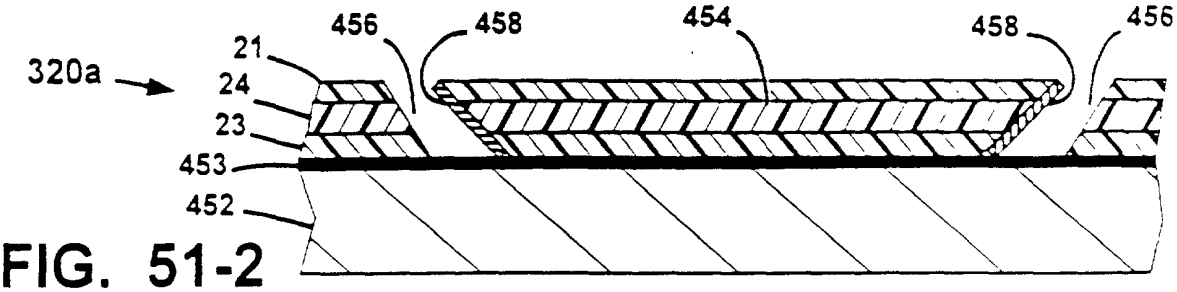


FIG._51-2

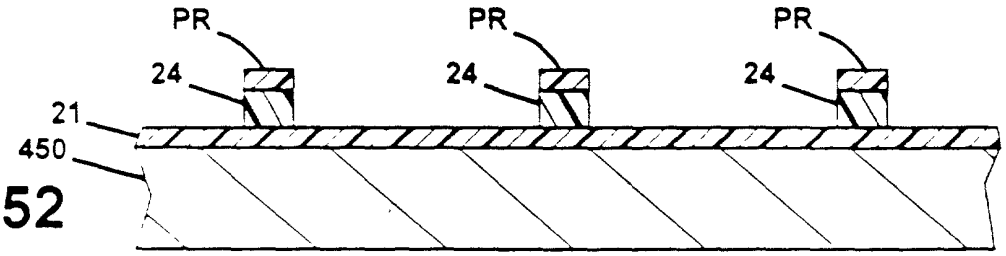


FIG._52

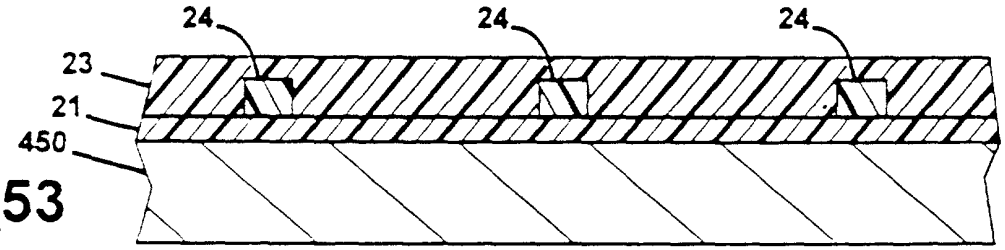


FIG._53

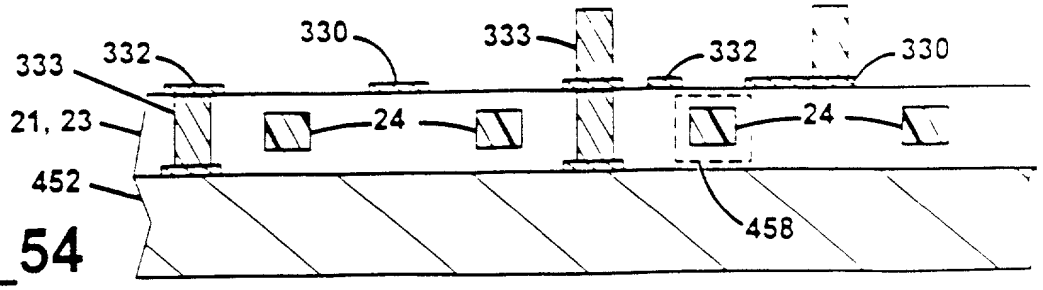


FIG._54

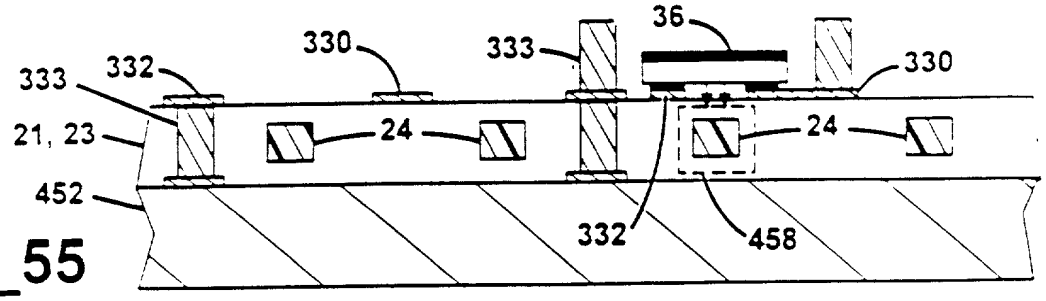


FIG._55

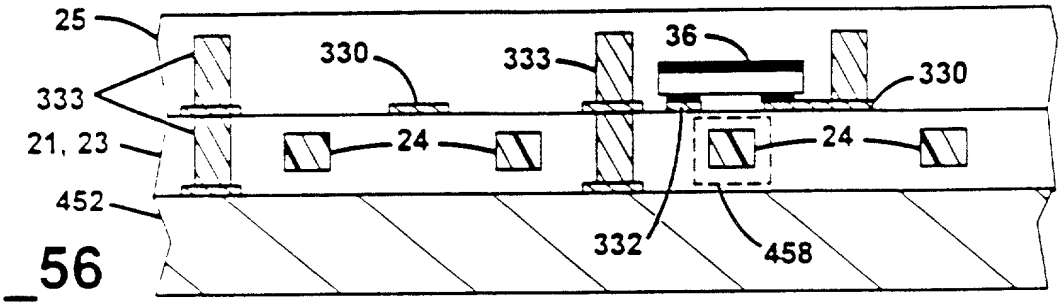


FIG._56

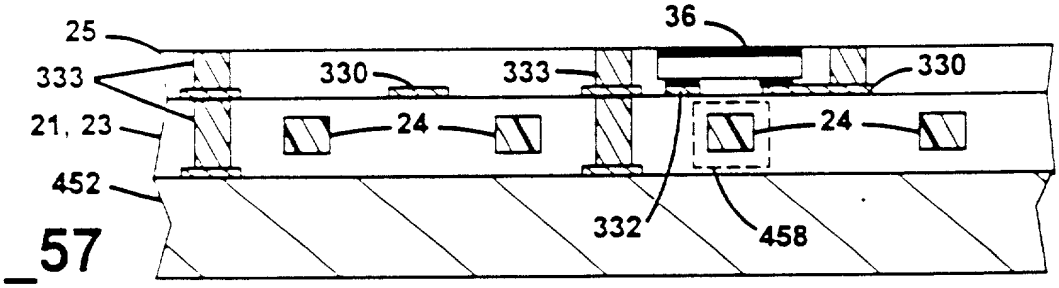


FIG._57

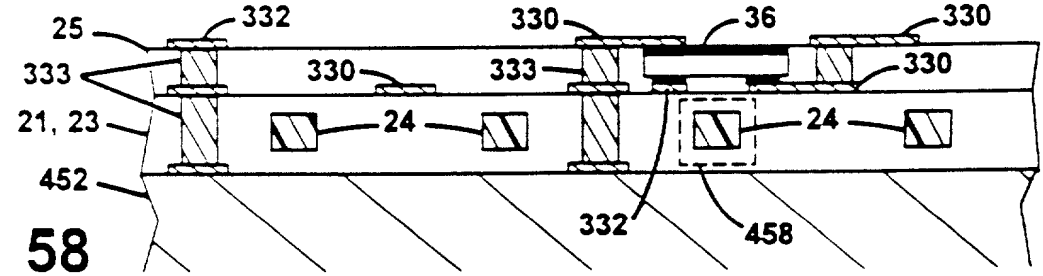


FIG. 58

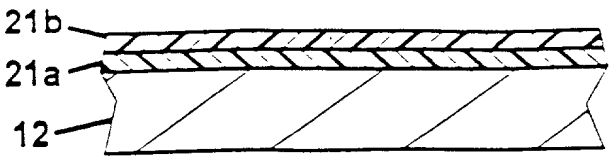


FIG._59

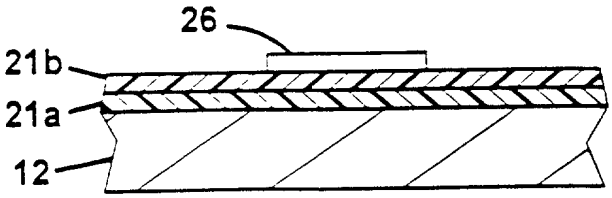


FIG._60

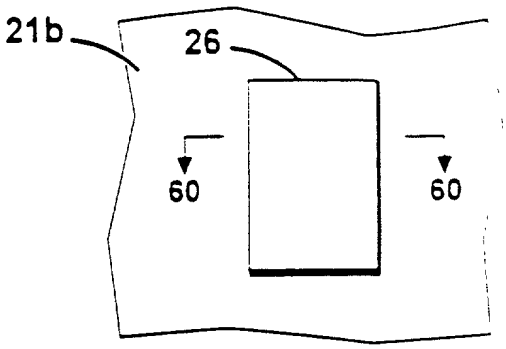


FIG._61

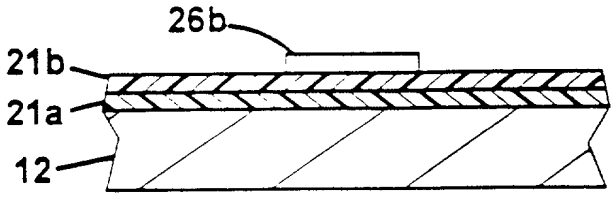


FIG._62

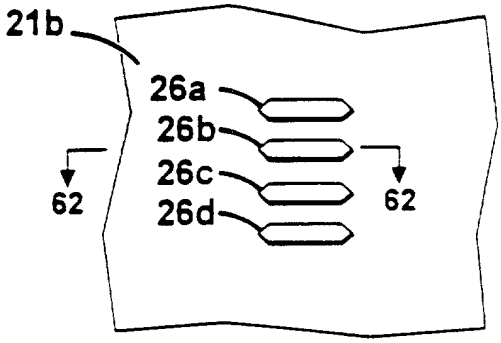


FIG._63

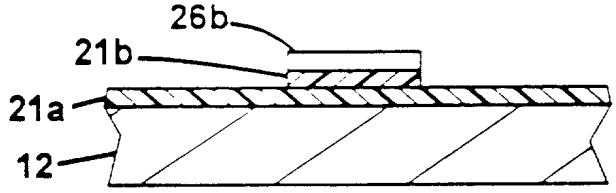


FIG._64

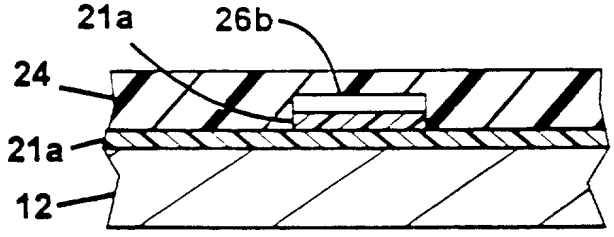


FIG._65

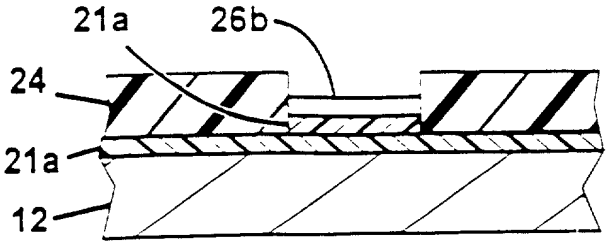


FIG._66

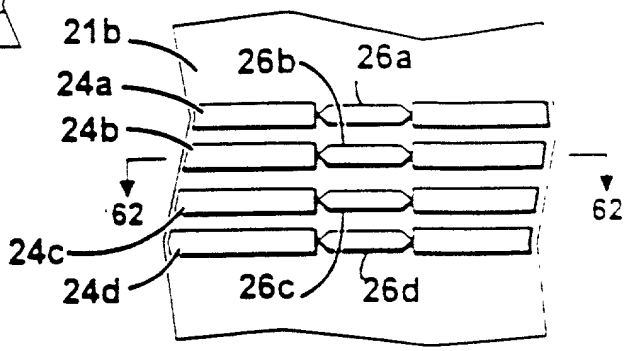


FIG._67

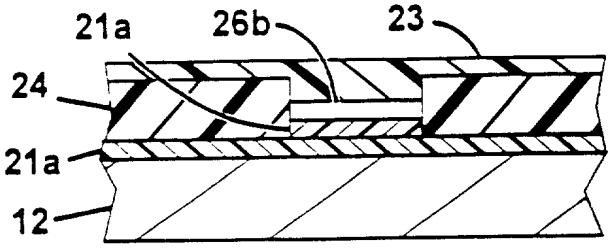


FIG._68

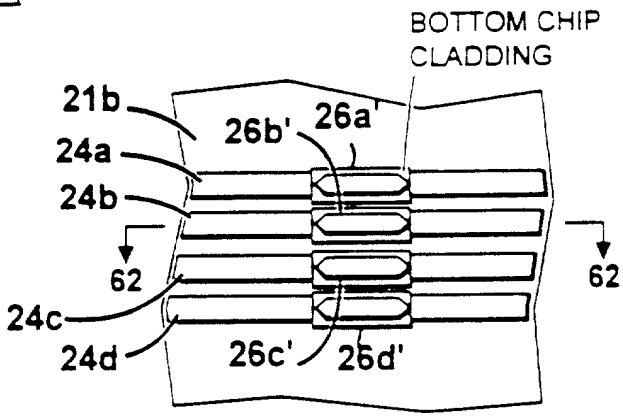


FIG._67-2

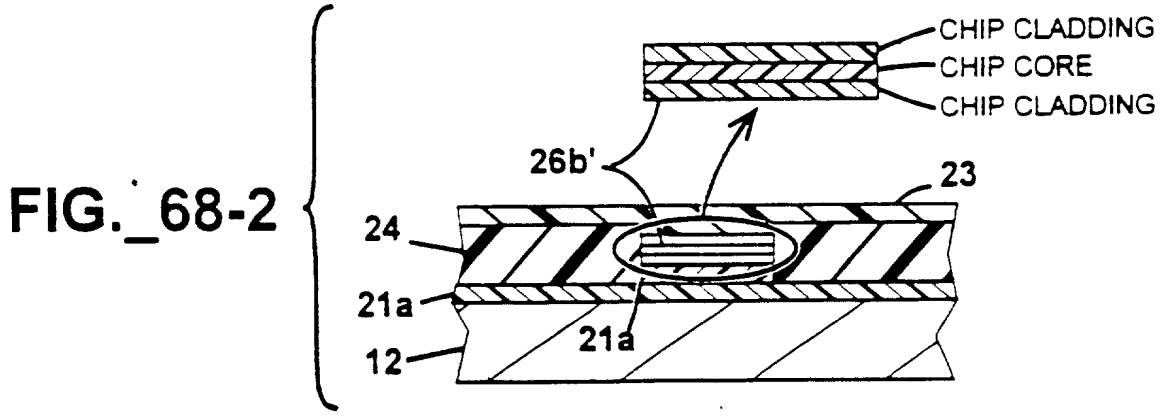


FIG._68-2

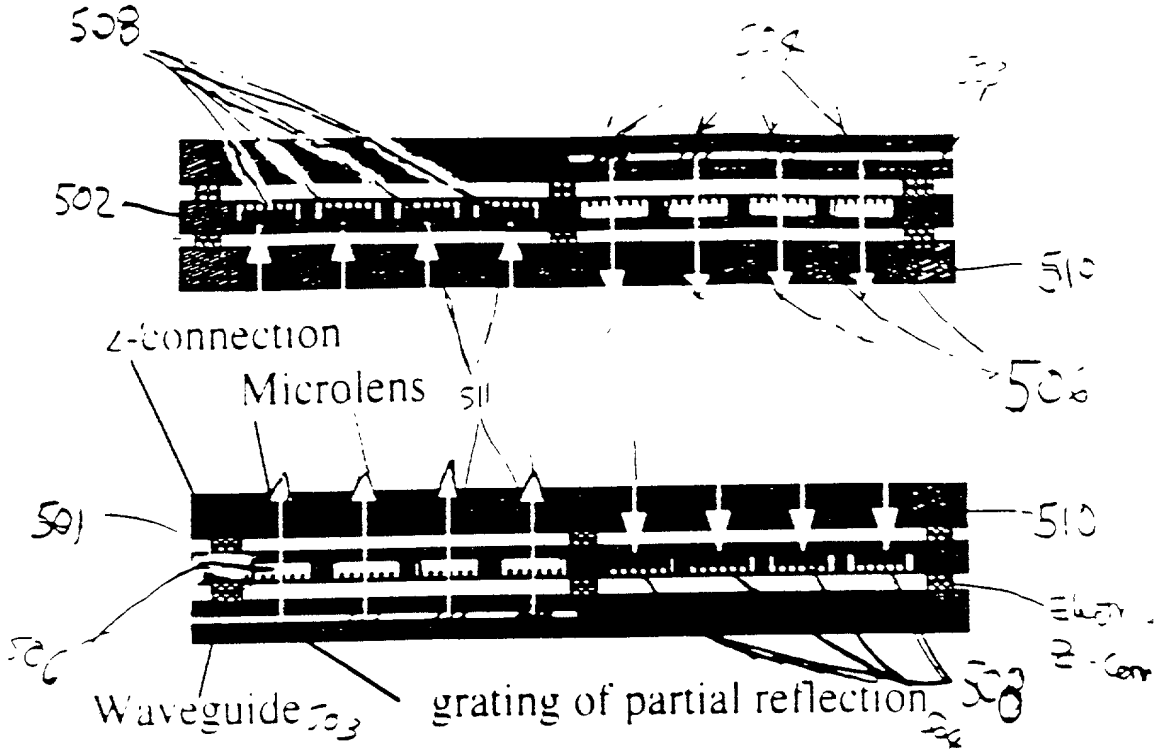

508
502
510
Z-connection
Microlens
511
501
510
Waveguide
grating of partial reflection

FIG. 5B

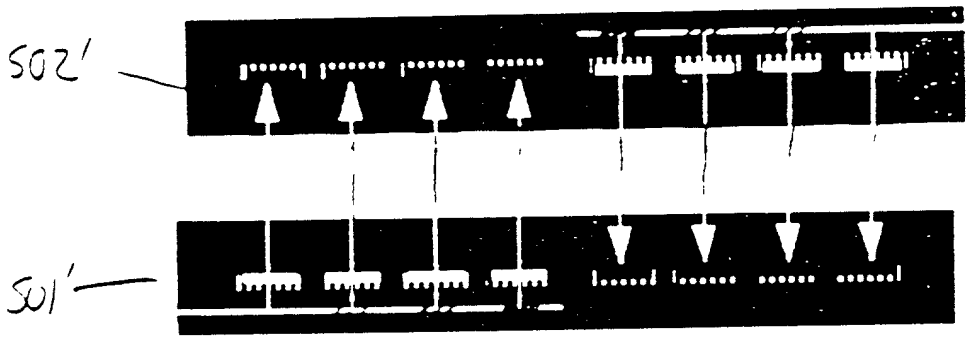

502'
501'

FIG. 7D

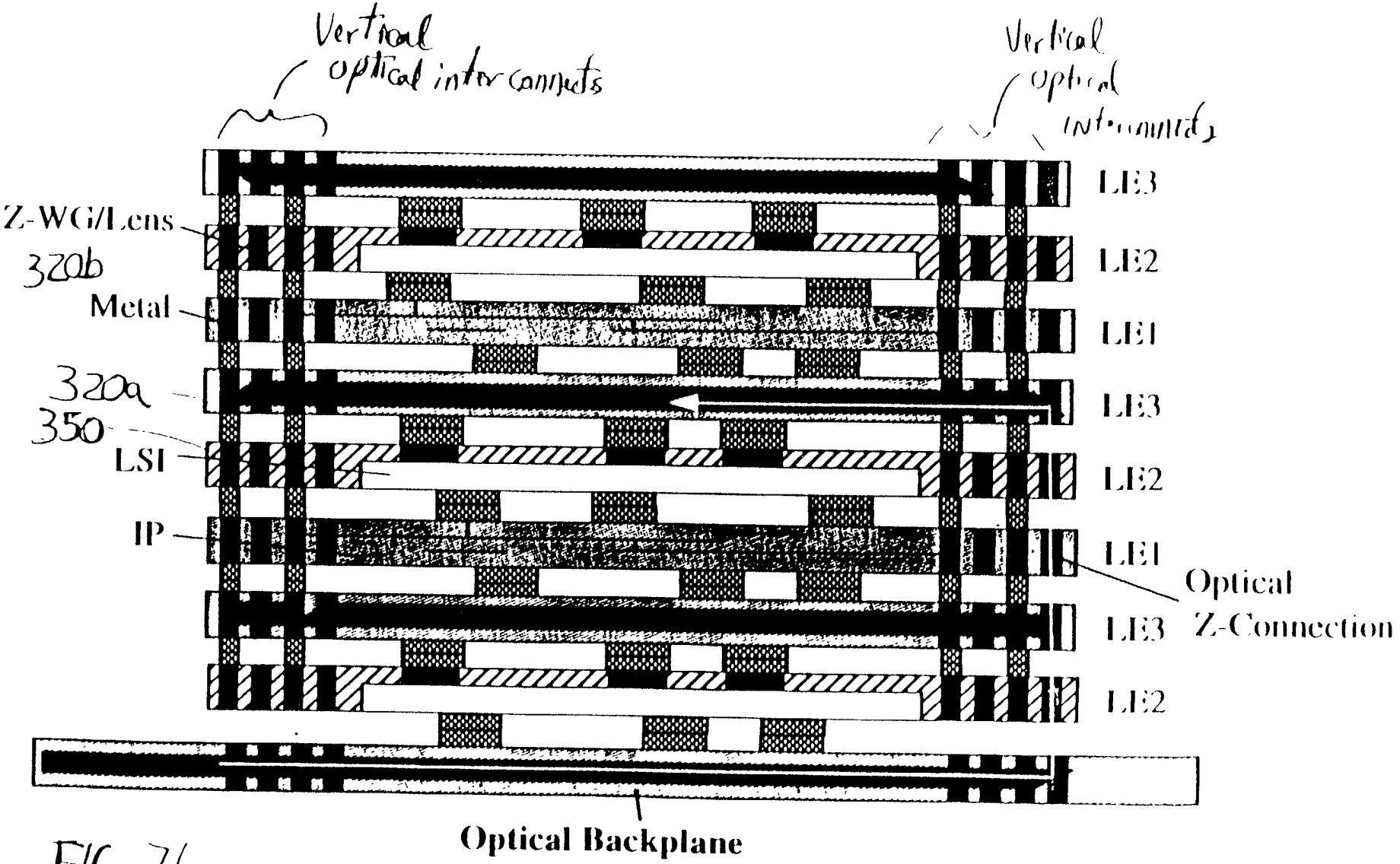
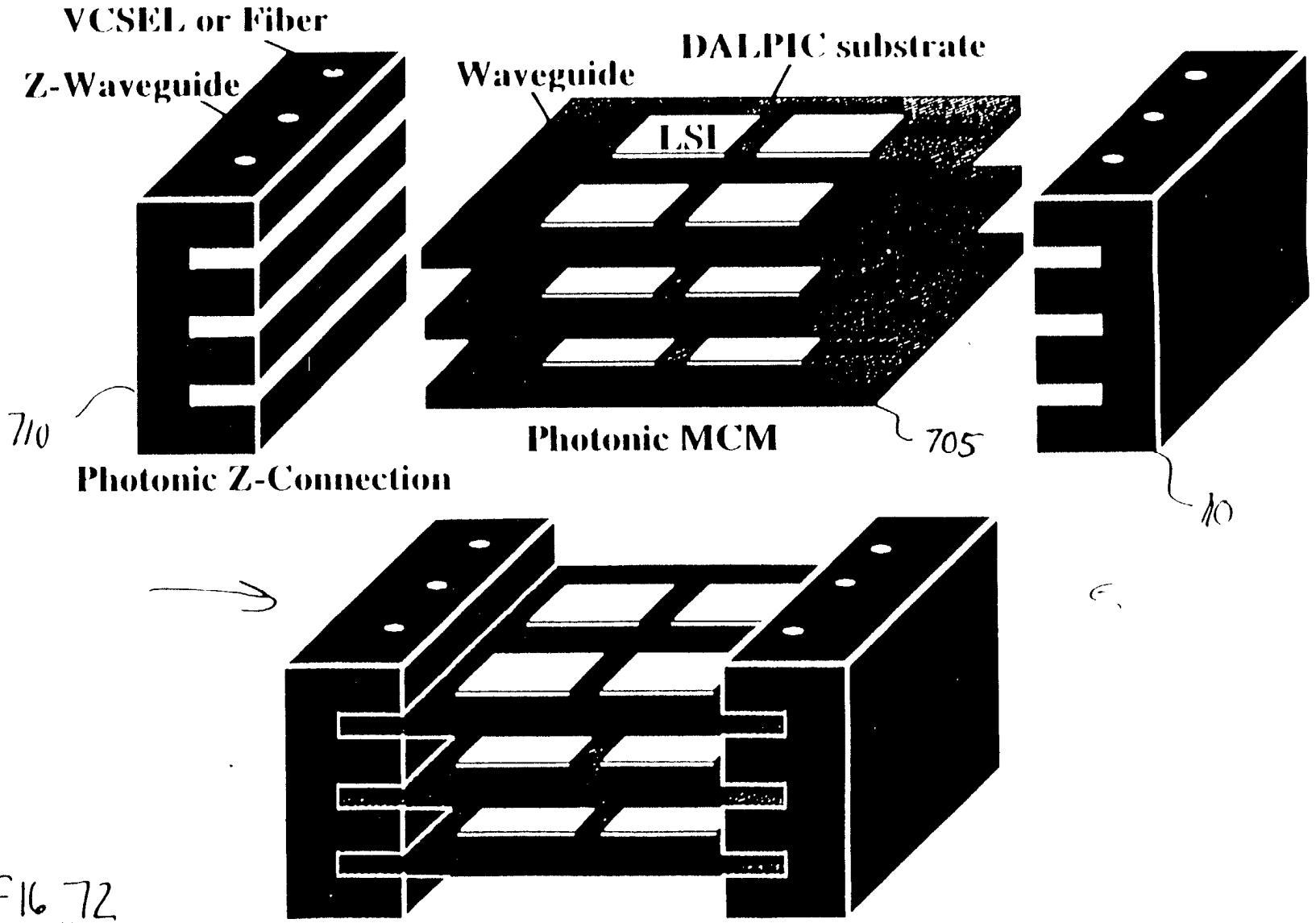


FIG. 7



F16 72

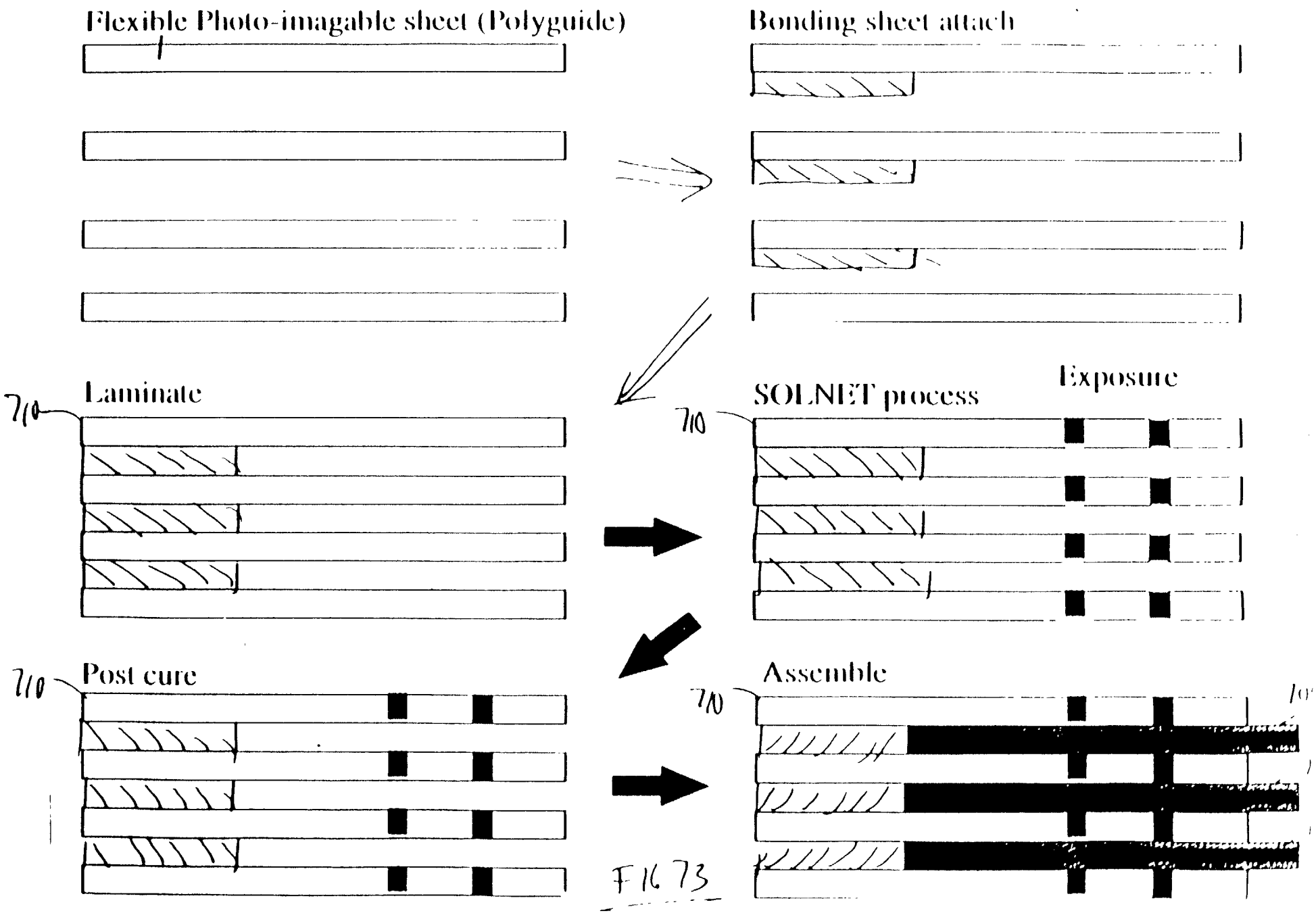


FIG 73

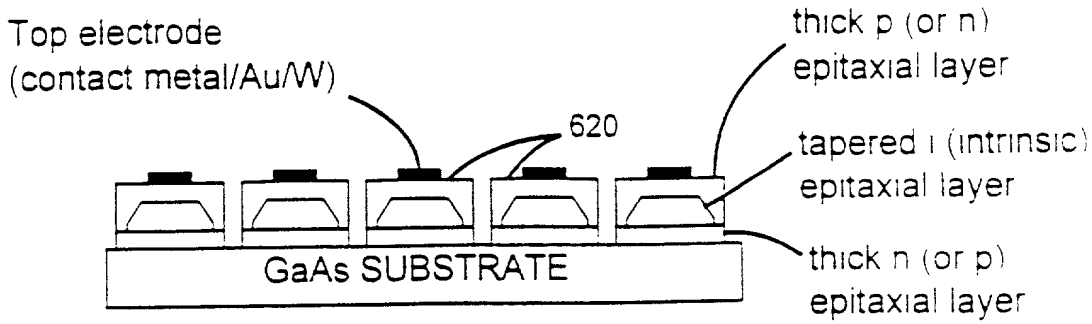


FIG._74 (Epitaxial growth and patterning)

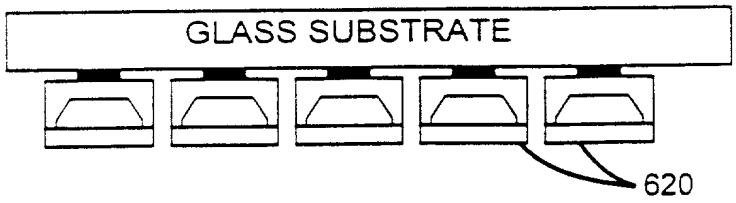


FIG._75 (Epitaxial liftoff)

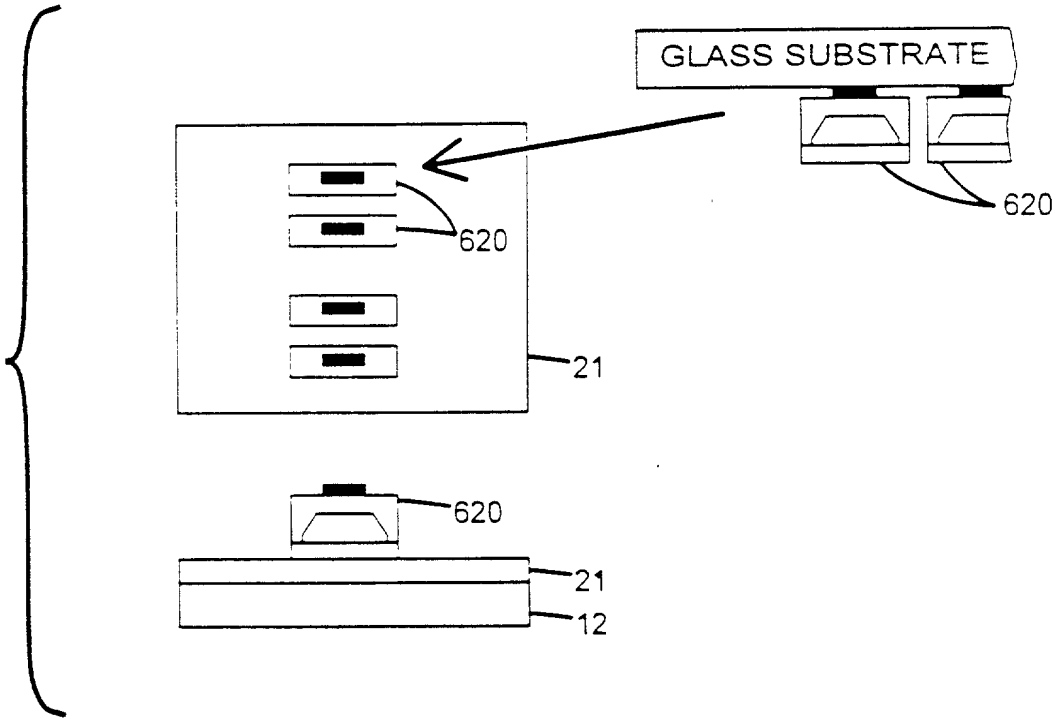
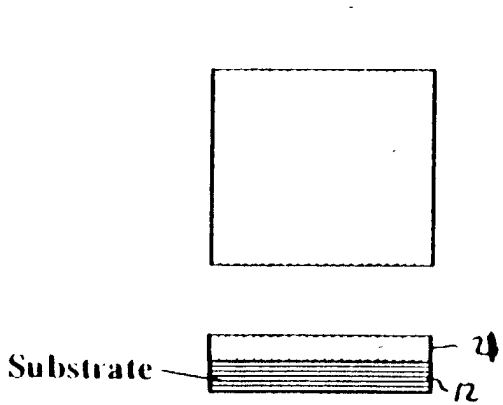
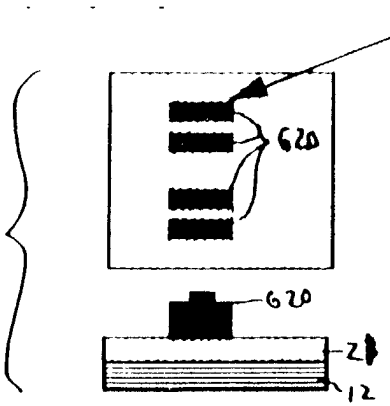


FIG._76 (Transfer)

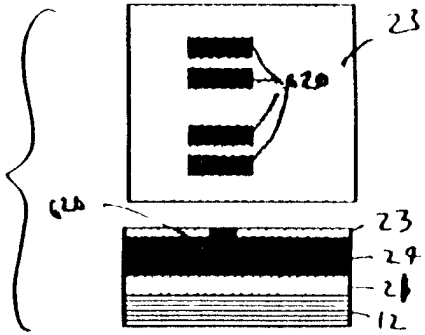


Underclad coat



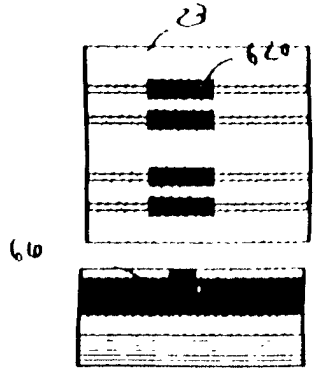
Thin-film device attatch

F16. 76



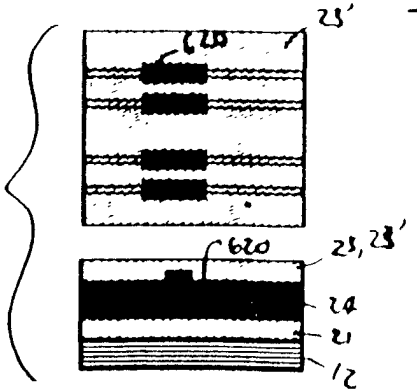
Core coat/Clad coat /CMP

F16. 77

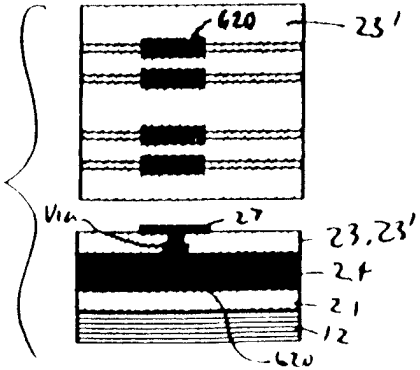


Core patterning

F16. 78

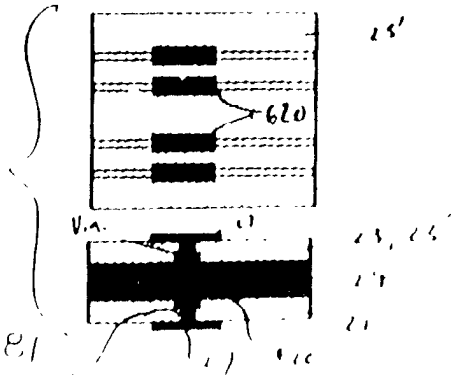


Clad coat



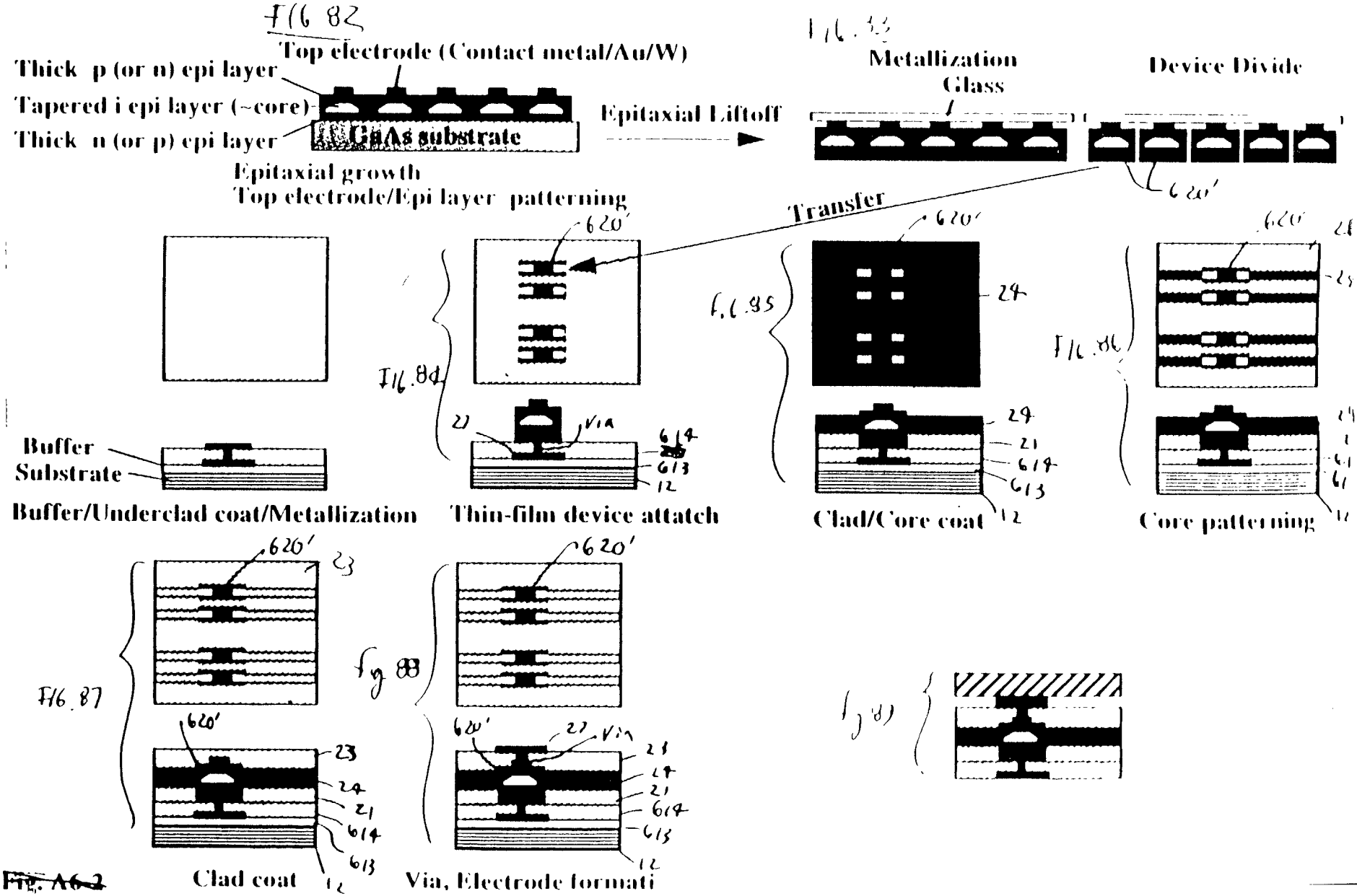
Via, Electrode formation

A6



F16. 81

Substrate



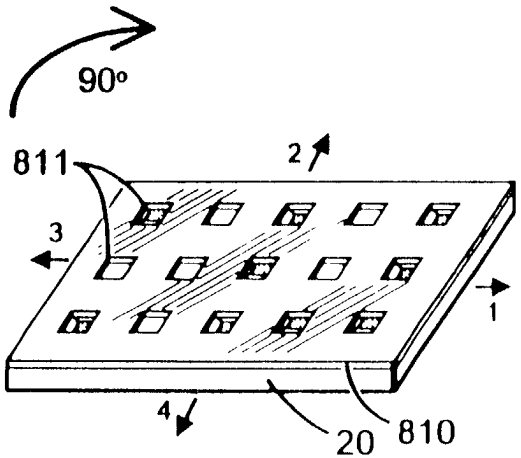


FIG._96

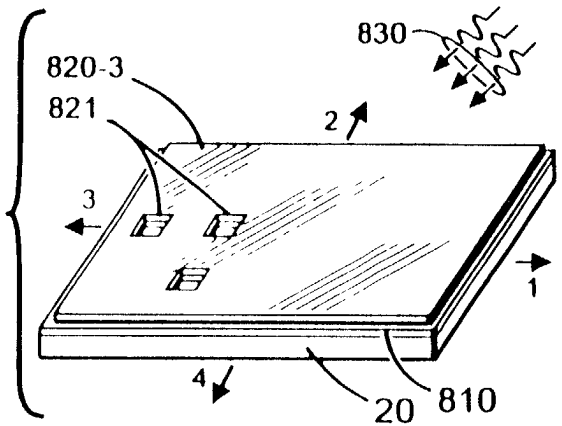


FIG._97

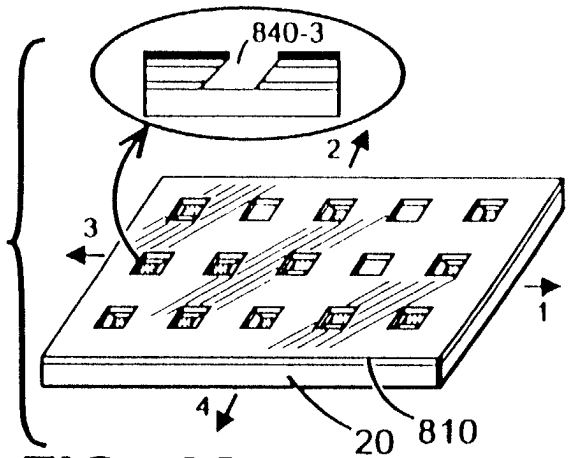


FIG._98

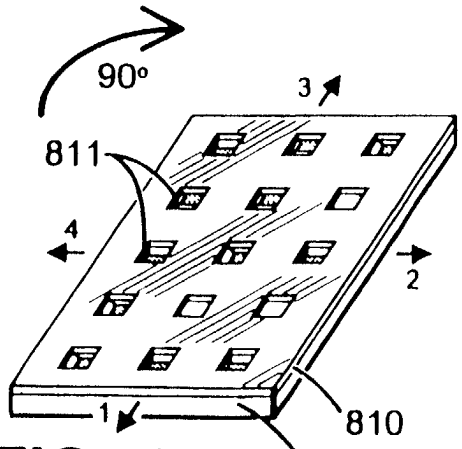


FIG._99

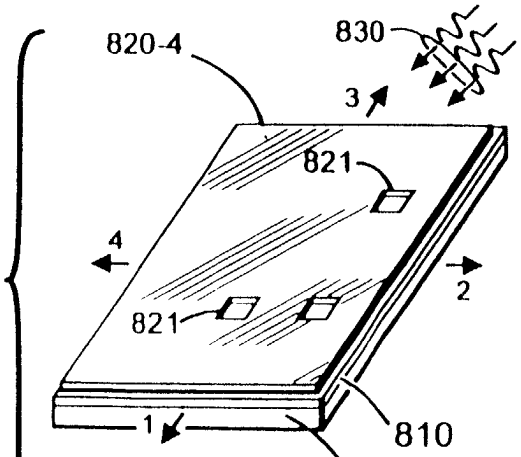


FIG._100

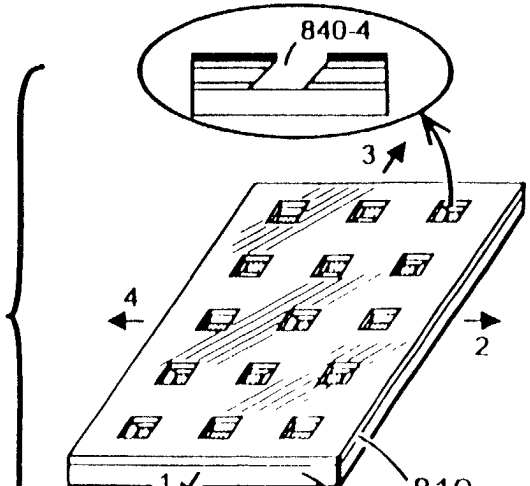


FIG._101

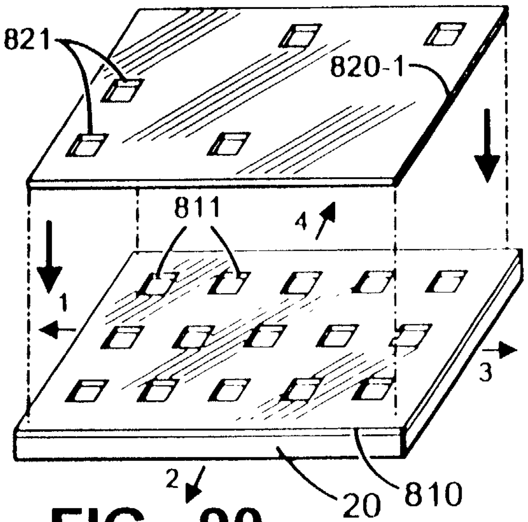


FIG._90

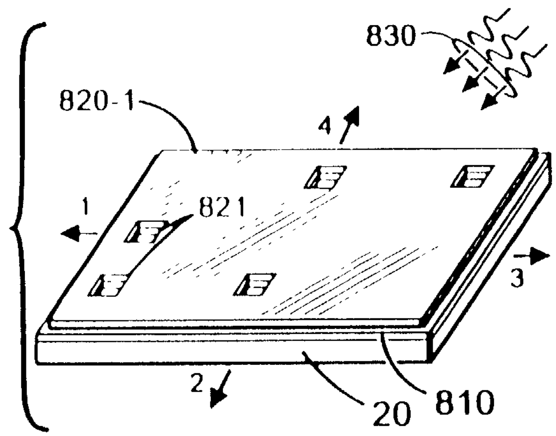


FIG._91

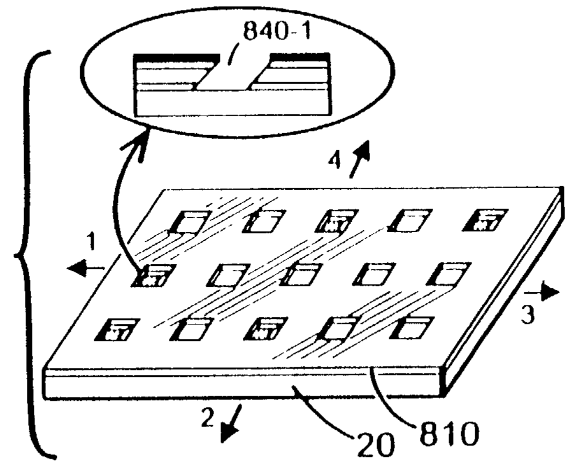


FIG._92

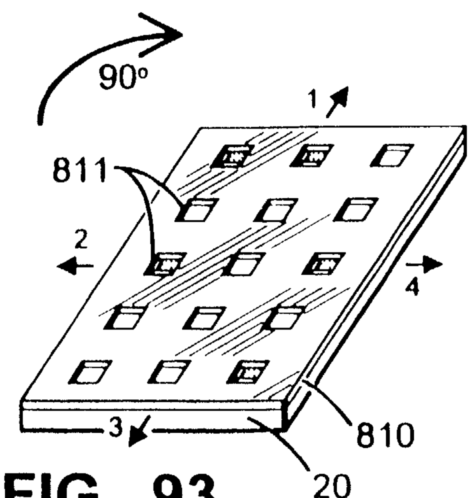


FIG._93

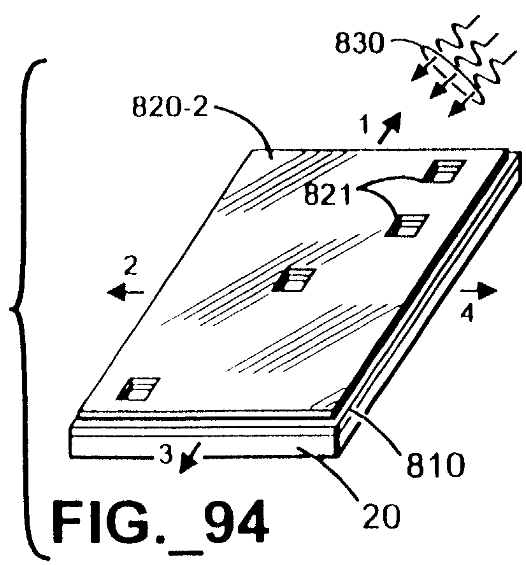


FIG._94

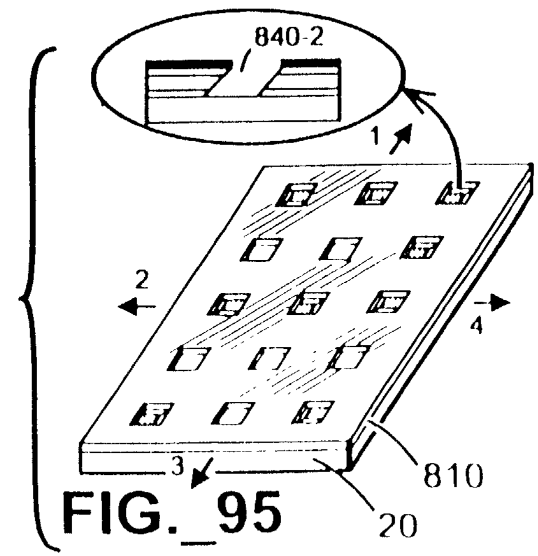


FIG._95

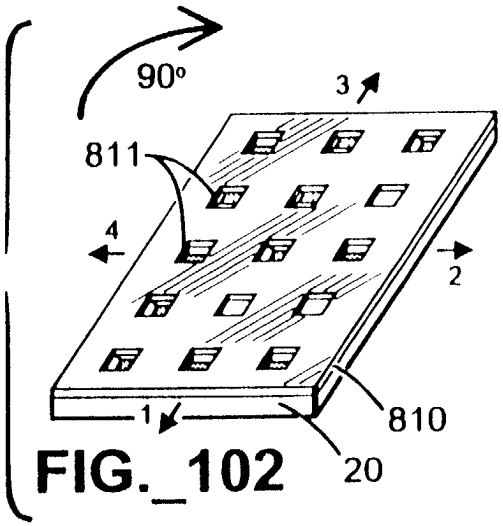


FIG._102

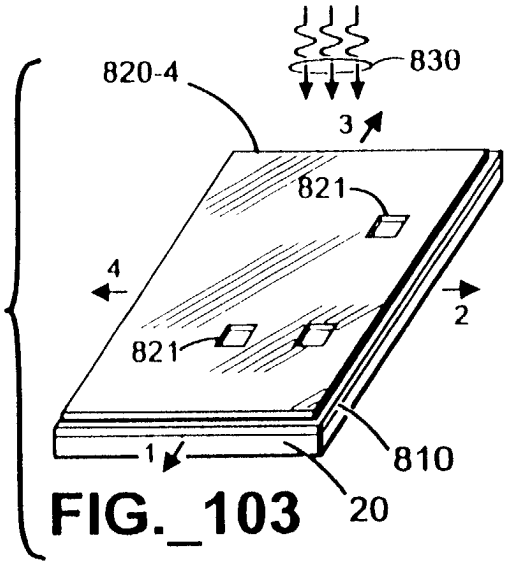


FIG._103

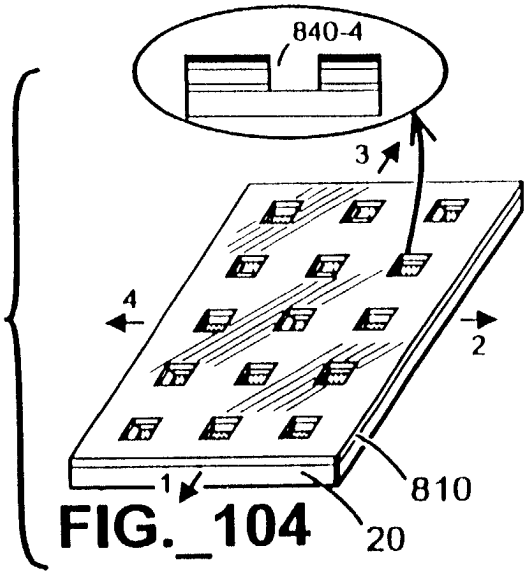


FIG._104

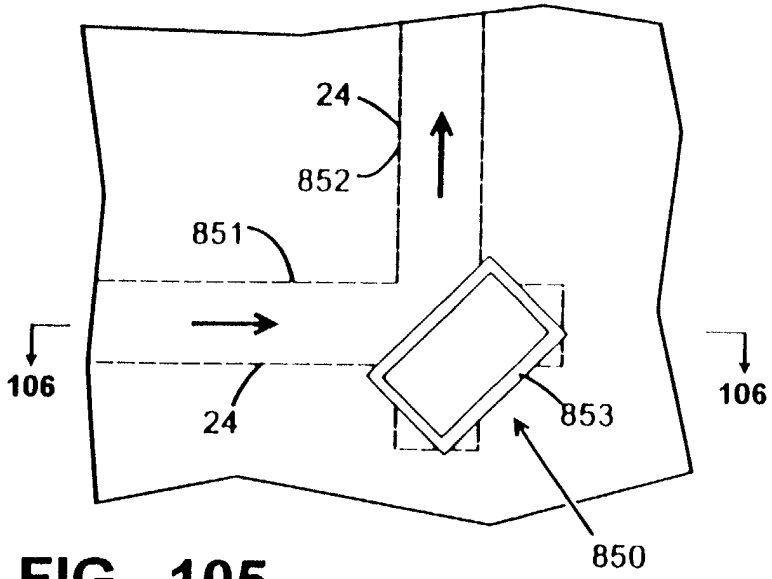


FIG._105

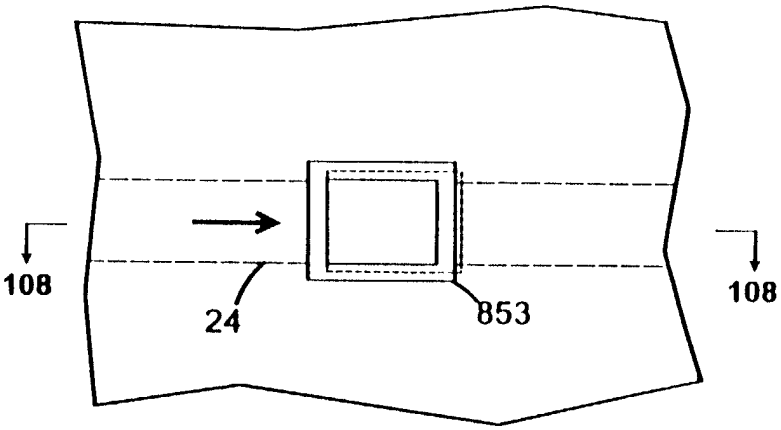


FIG._107

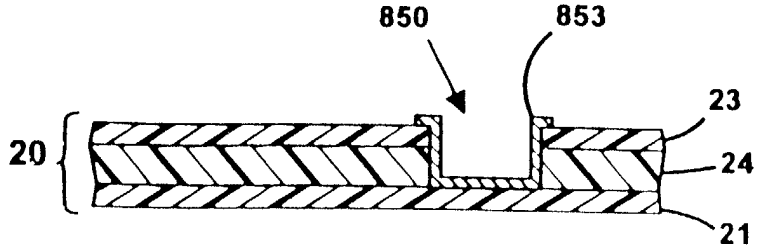


FIG._106

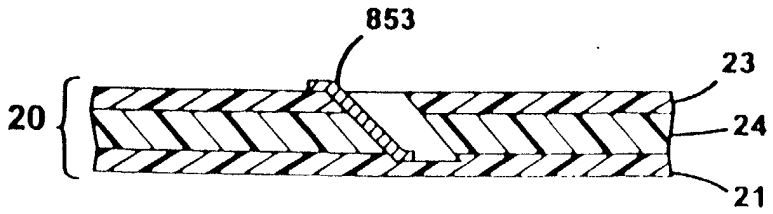


FIG._108

FUJITSU Computer Packaging Technologies, Inc. FCPT

GS CX/CXX OE Solution --- OE-3D-Stack

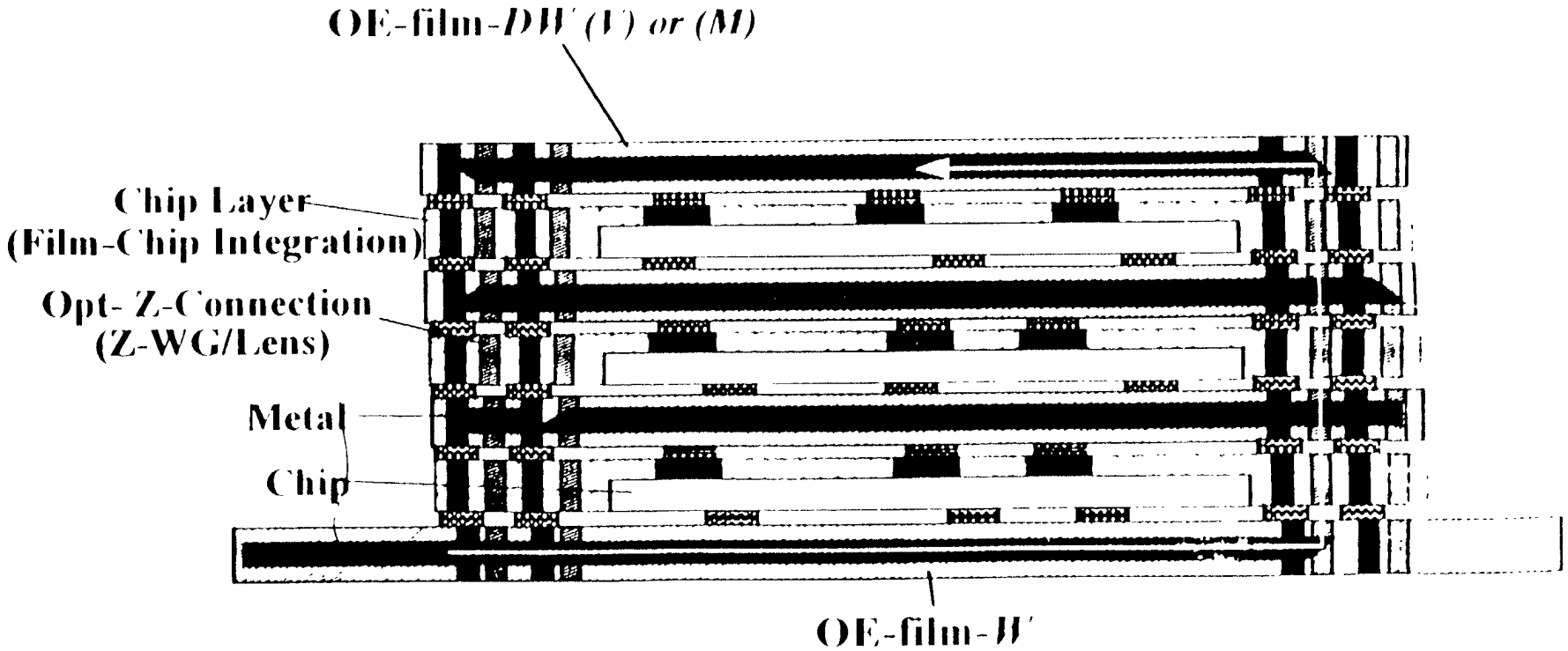


FIG. 109

A22

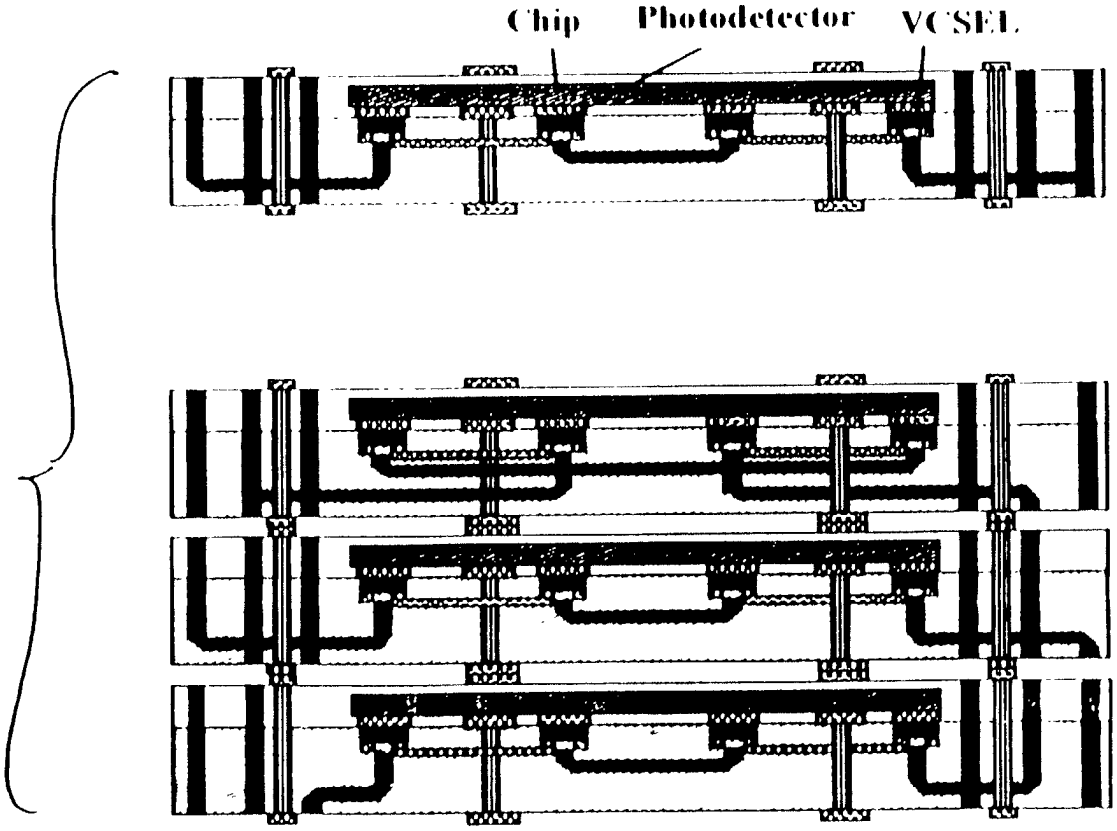


FIG. 11O

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

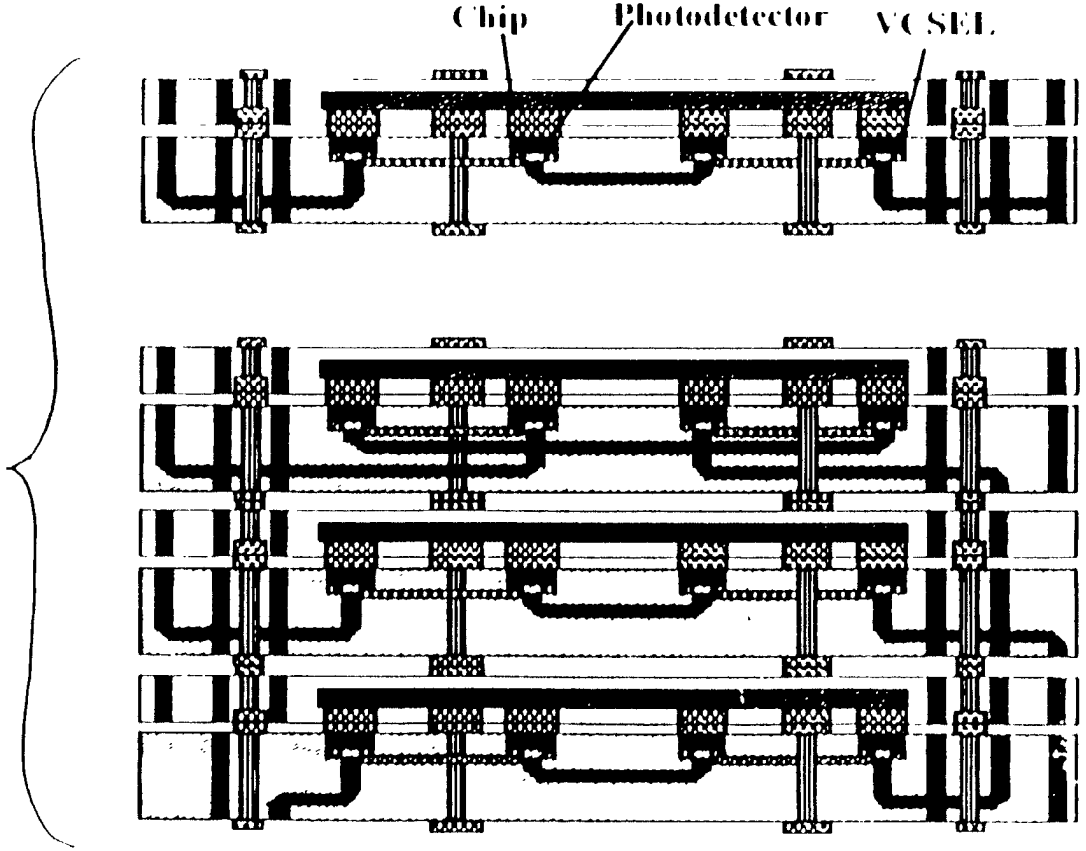


FIG. 11A

A24

(2/23/99) AA2 Detail picture Example for 3D-stack'

(New version of the AA2 of 2/5/99)

Film/Z-Connection Application to OE-Substrate

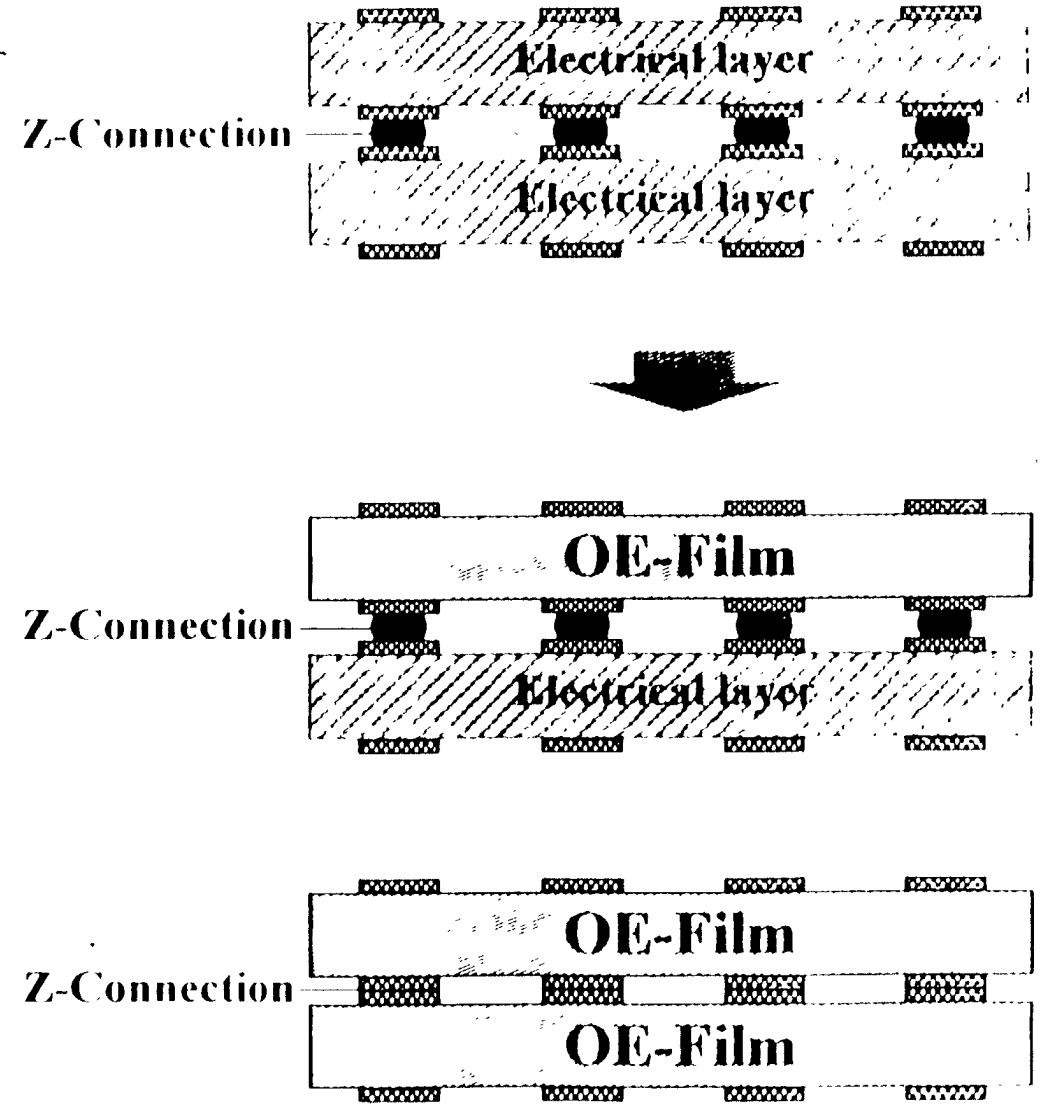


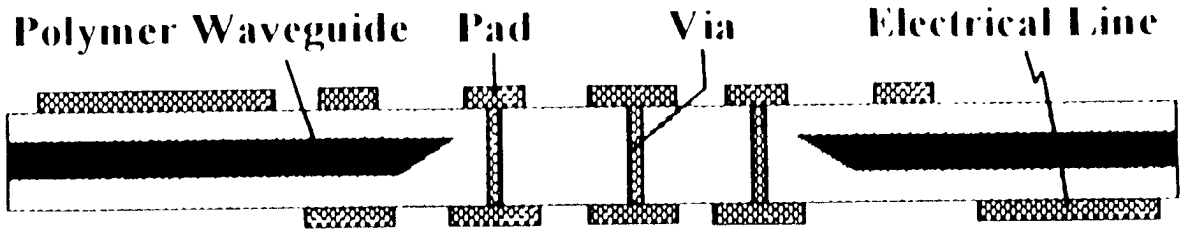
FIG. 1/2

A7

2/23/99-added 1

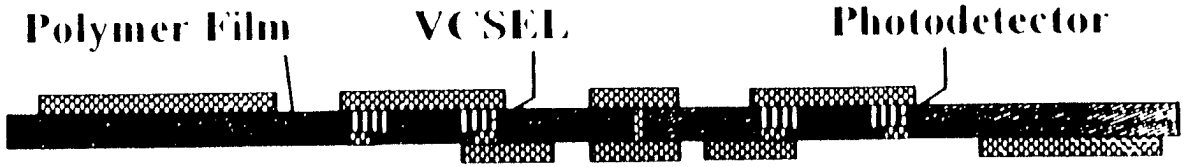
OE-Films

OE-film-*W*



F16.113

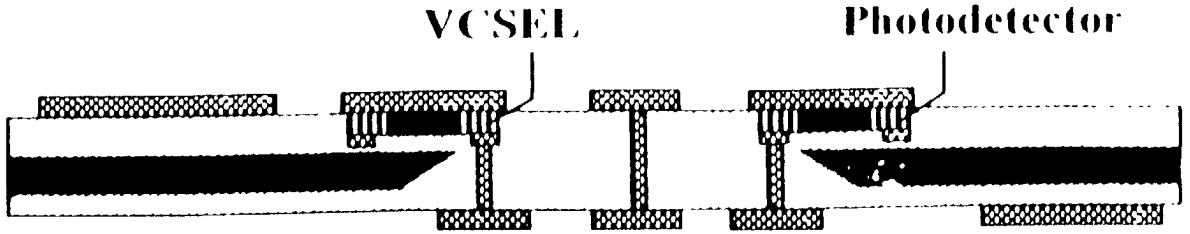
OE-film-*D*



F16.114

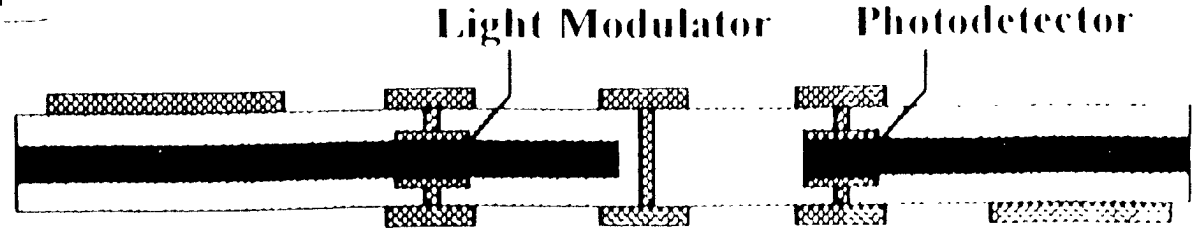
A8

OE-film-*DW(V)*



F16.115

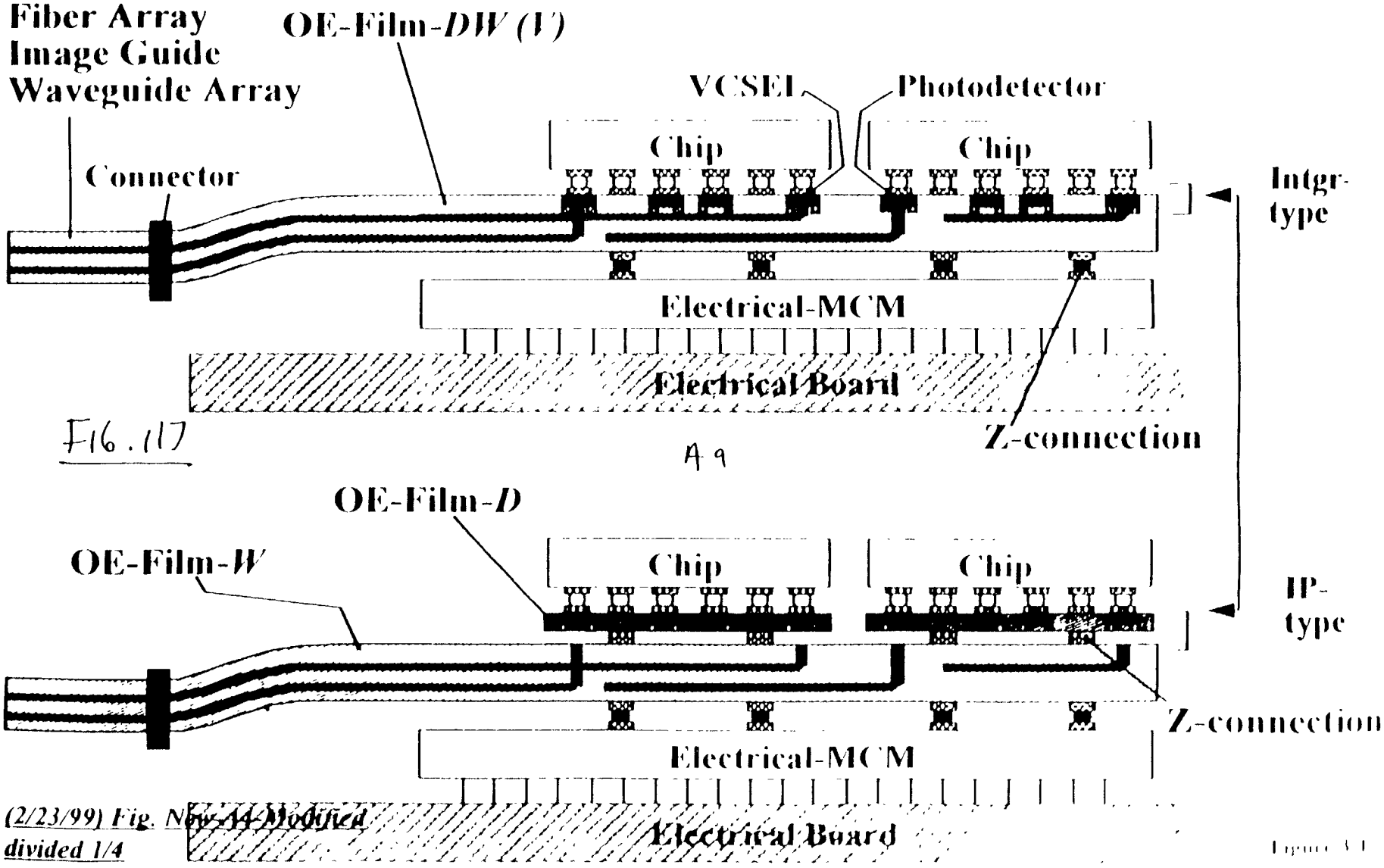
OE-film-*DW(M)*



2/17/99-added 2

F16.116

FOLM



F16.117

A 9

(2/23/99) Fig. New-14-Modified
divided 1/4

F16.118

FOLM

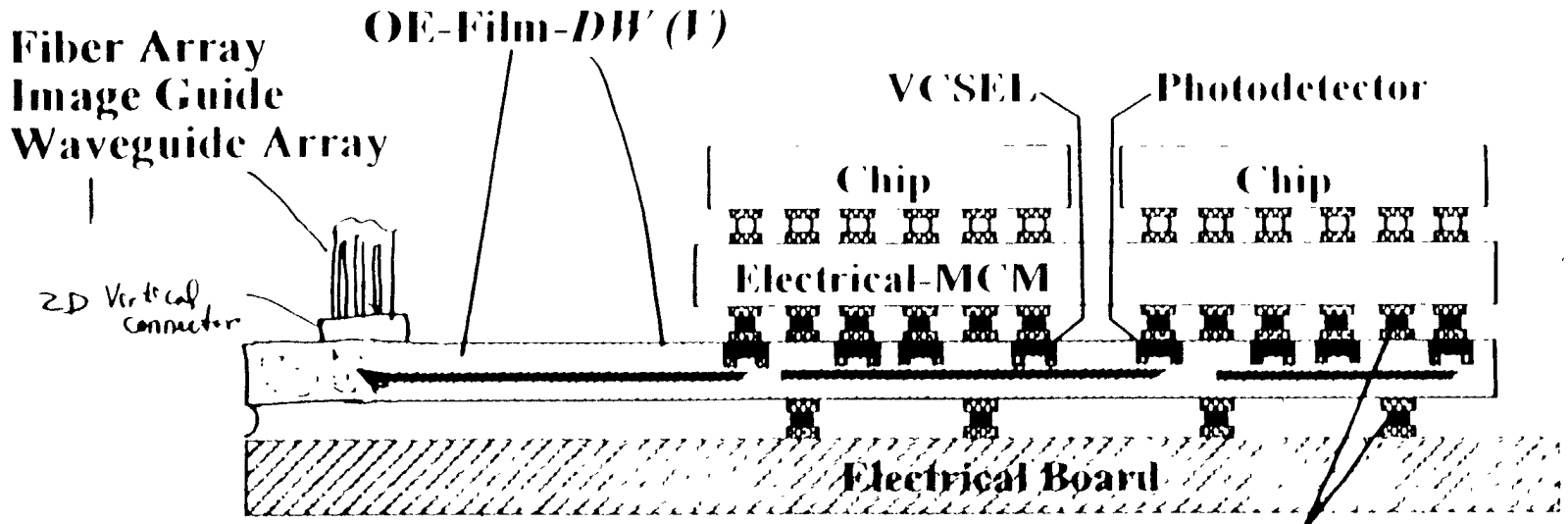
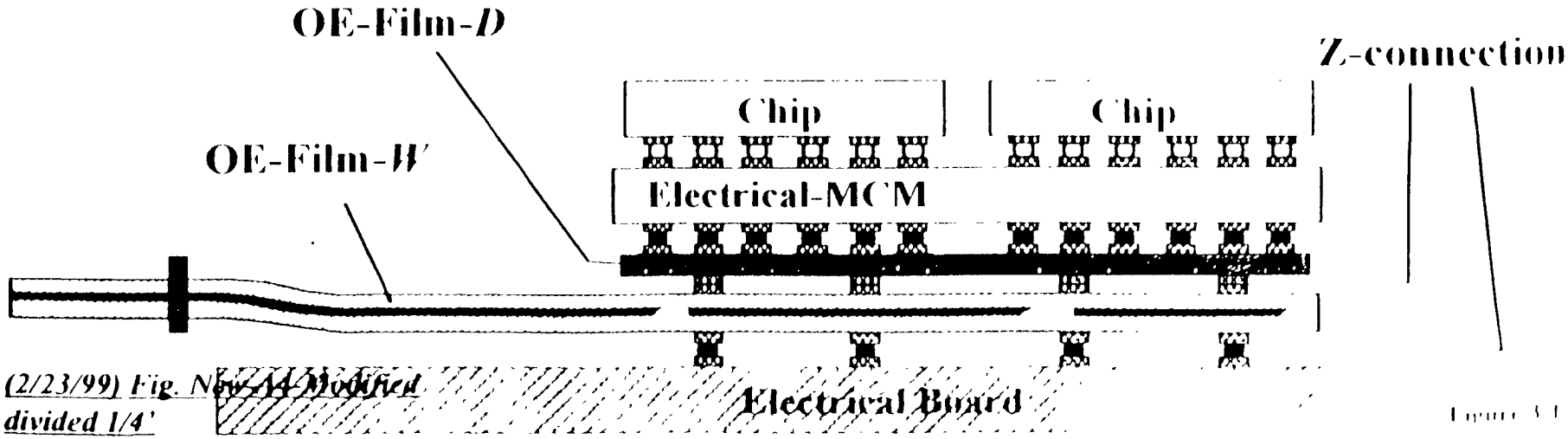


Fig. 119

A10

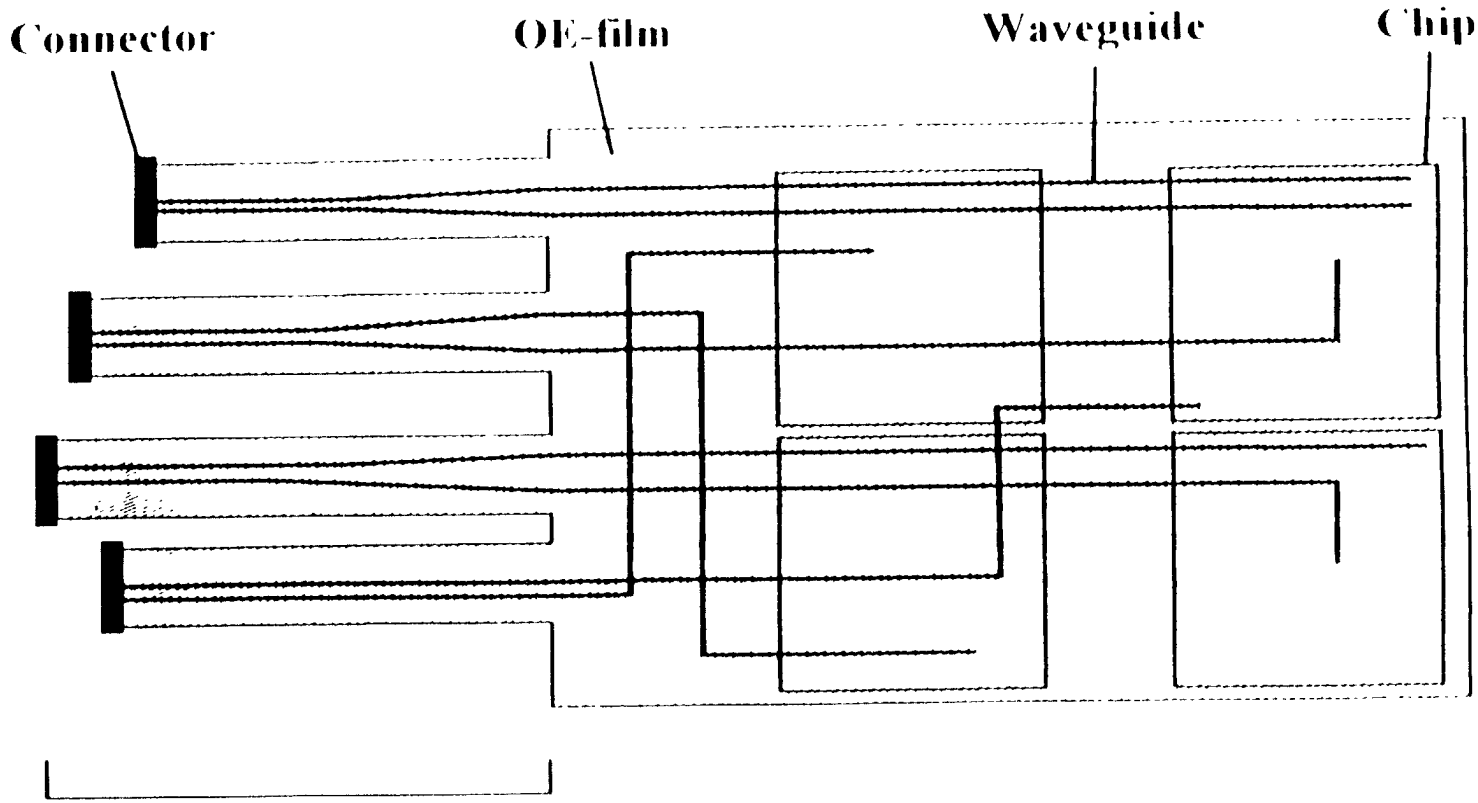


(2/23/99) Fig. New 14 Modified divided 1/4'

Fig. 120

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM with Optical Path Length Controller, Connector Buffer



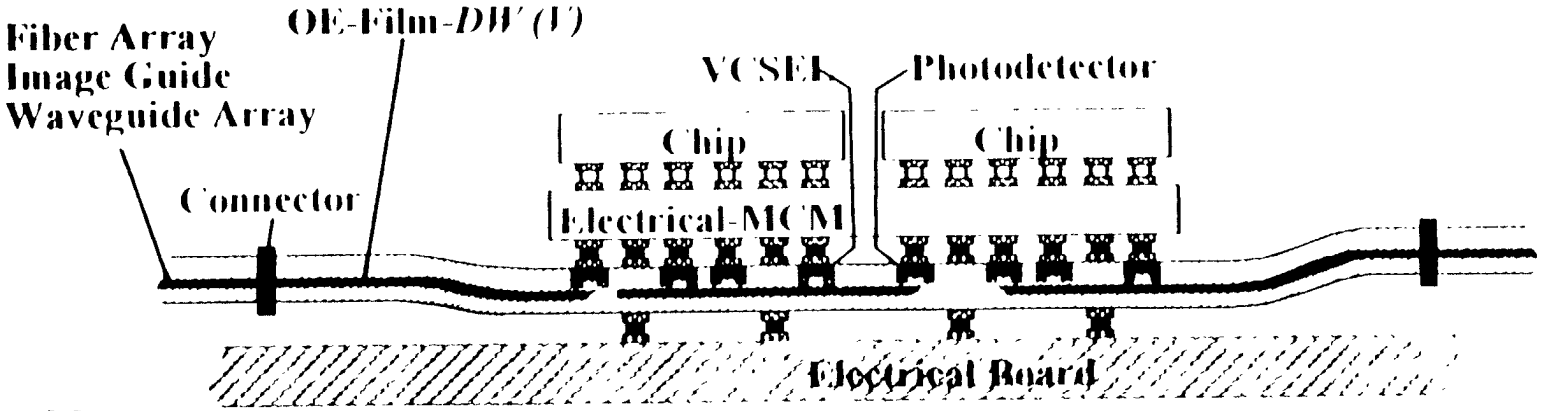
All

FIG. 12

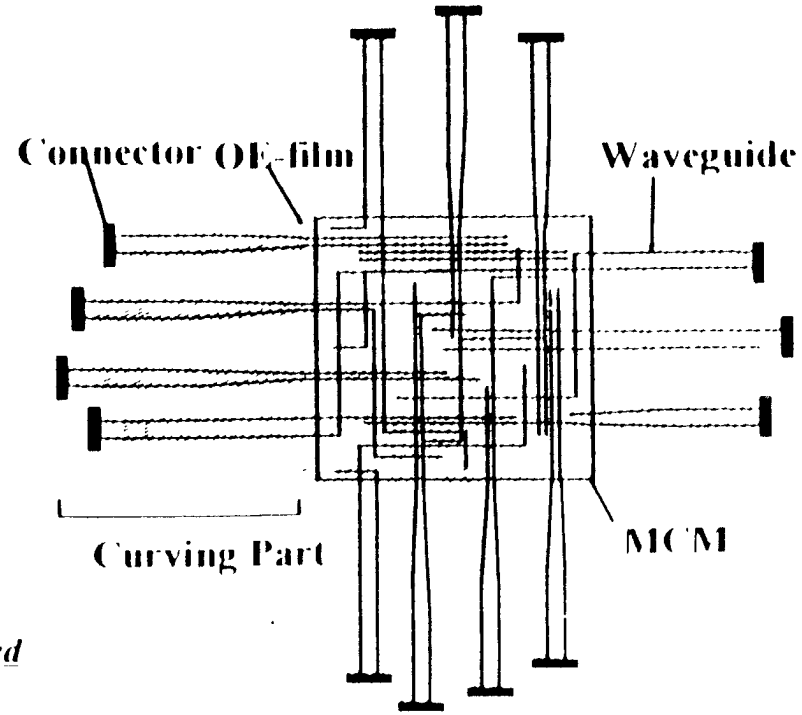
(2/17/99) Fig. New-A4-Modified
divided 2/4

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM with Optical Path Length Controller, Connector Buffer



F16. 123

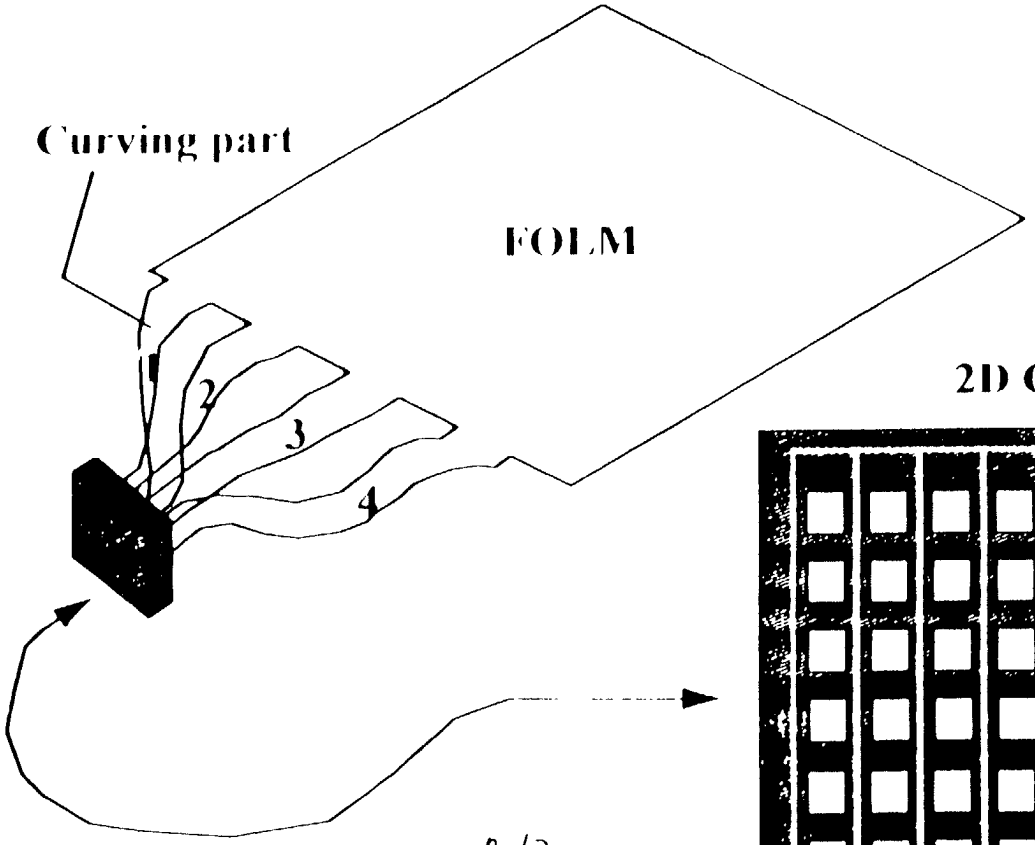


F16. 122

A12

(2/23/99) Fig. New-A4-Modified divided 2/4'

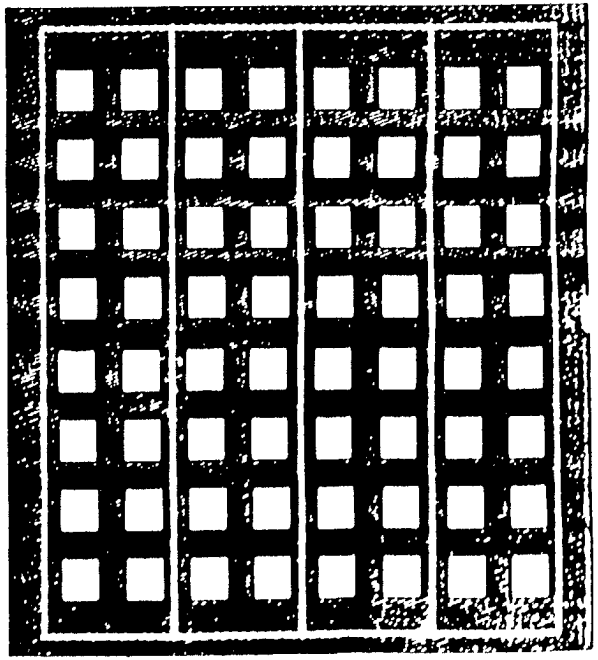
FOLM with 2D Waveguide Connector



A 13

FIG. 12A

2D Connector cross-section



core

(for Single-layer waveguide) (for 2 layer waveguide)

(2/23/99) Fig. New-A4-Modified divided 3/4'

FOLM: High-Speed Option

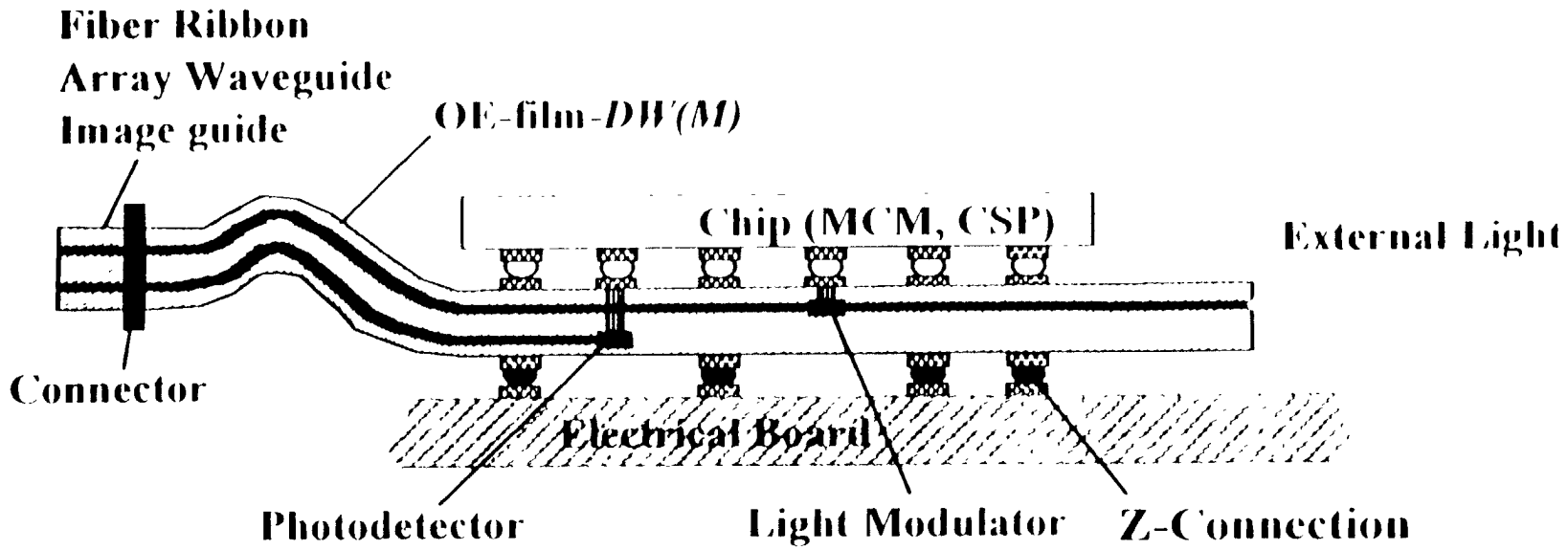


FIG. 12S

A 14

(2/17/99) Fig. New-A4-Modified
divided 4/4

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM Structure Example (Overall)

Through put: 1.5 pbs x 196 ch Assume SSX MCM Size is ~5 cm x 5 cm Unit: um

Fig. 126

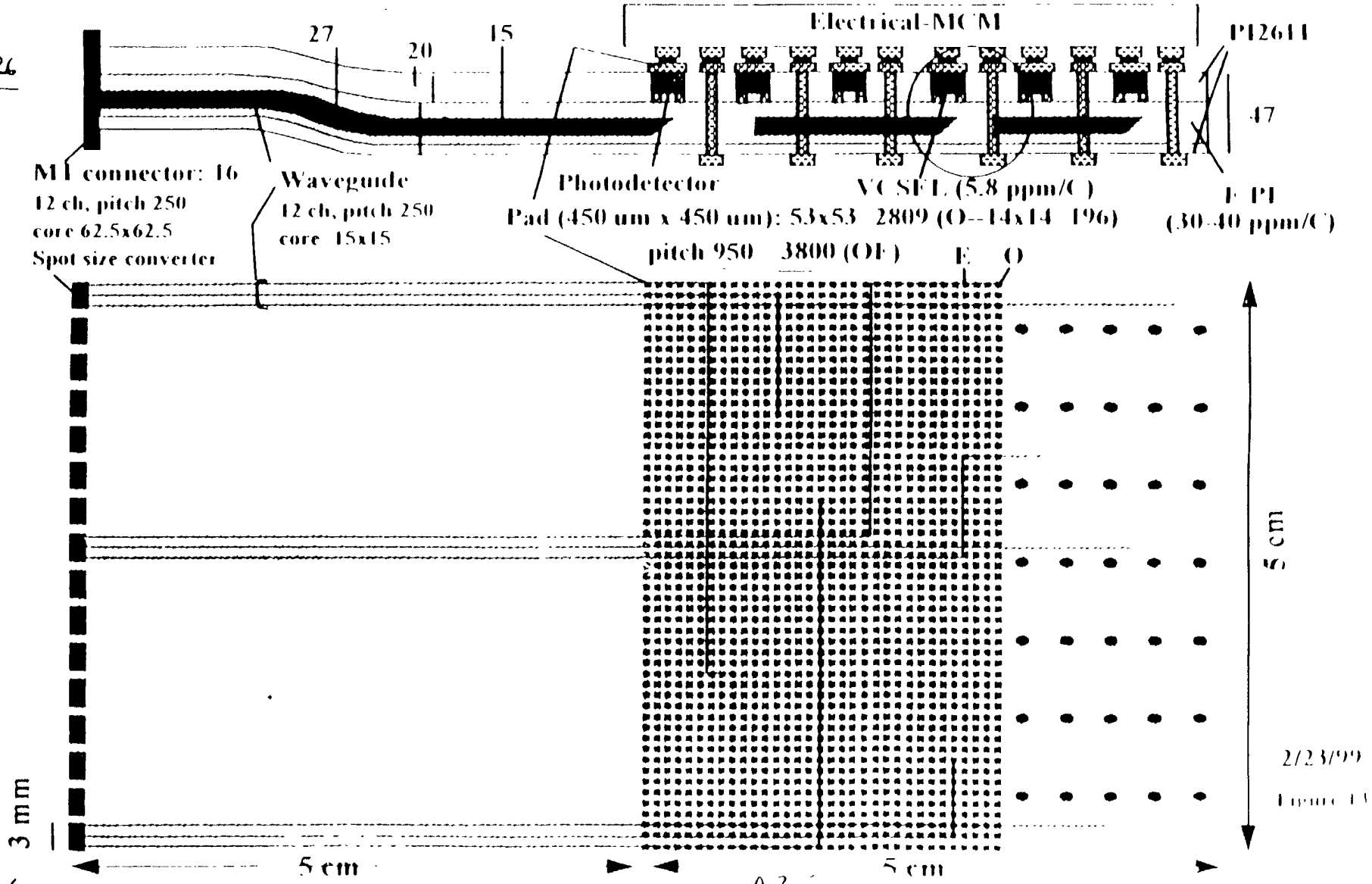
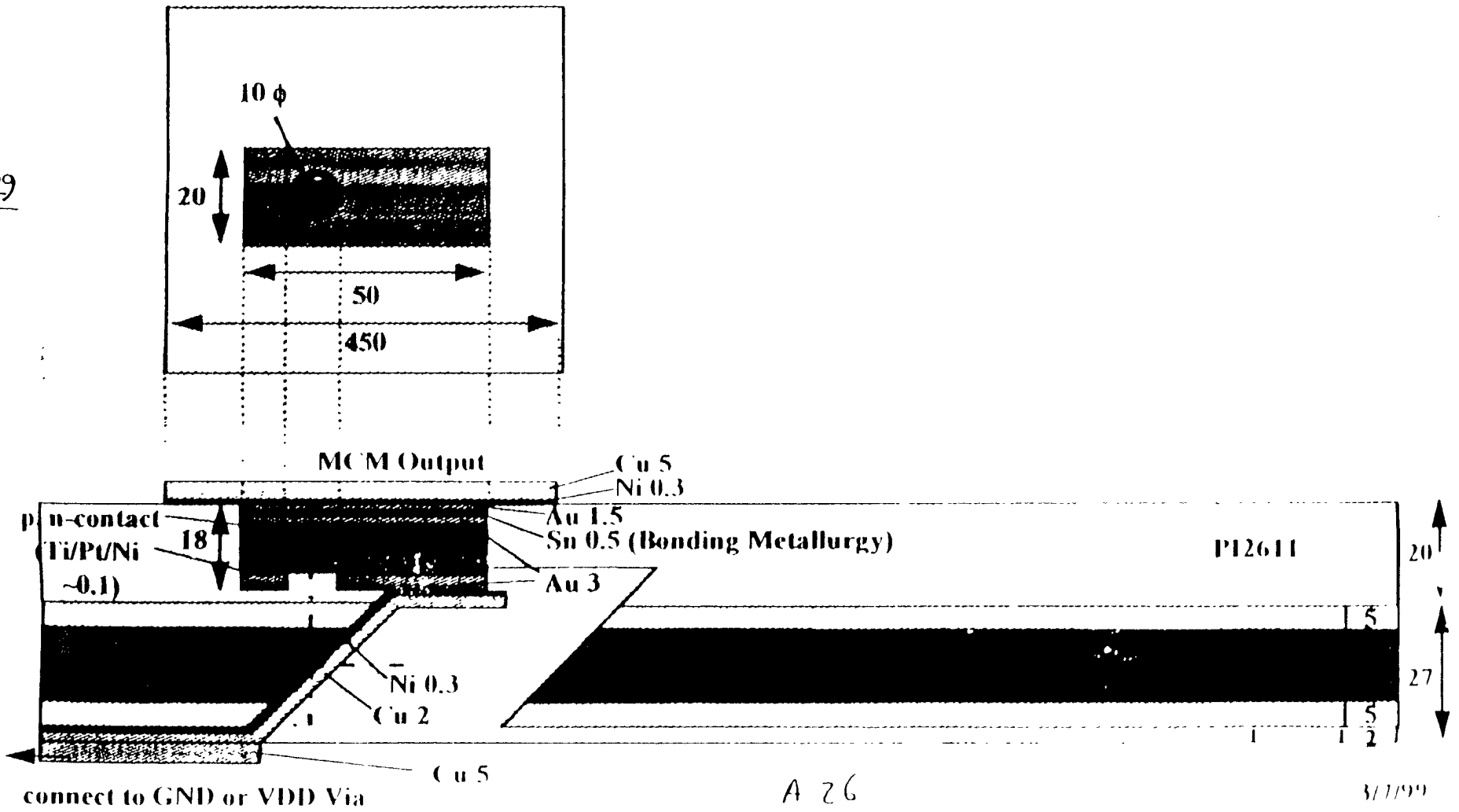


Fig. 127

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM Structure Example (VCSEL part)

FIG. 129



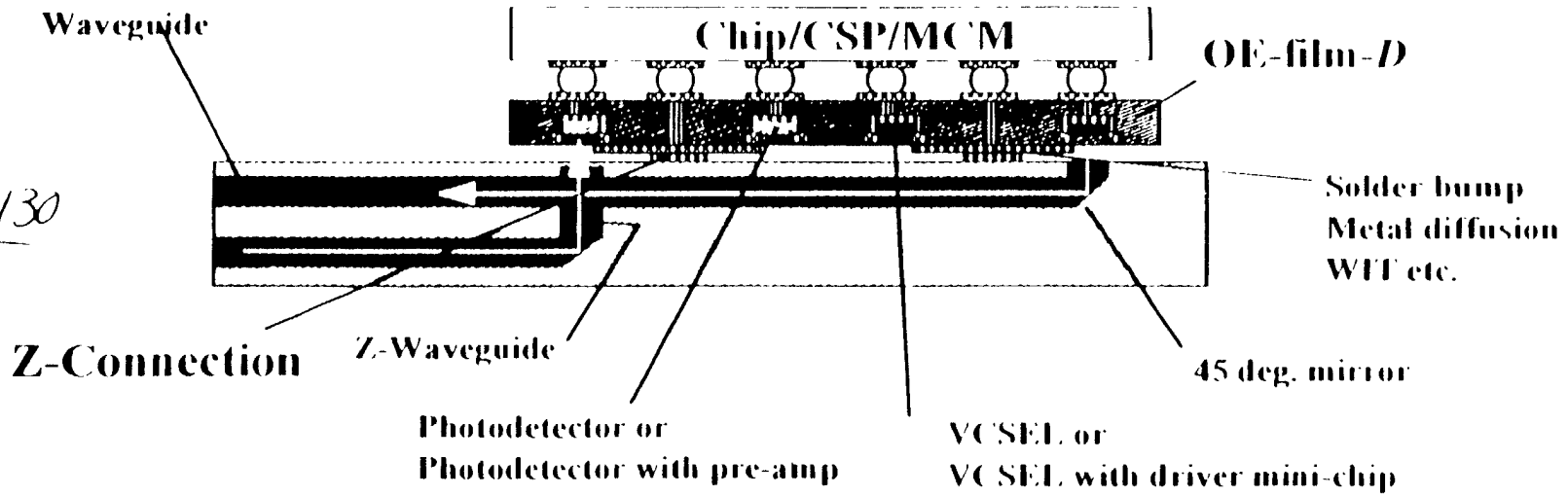
A 26

FIG. 128

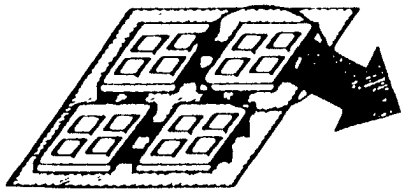
Unit : um

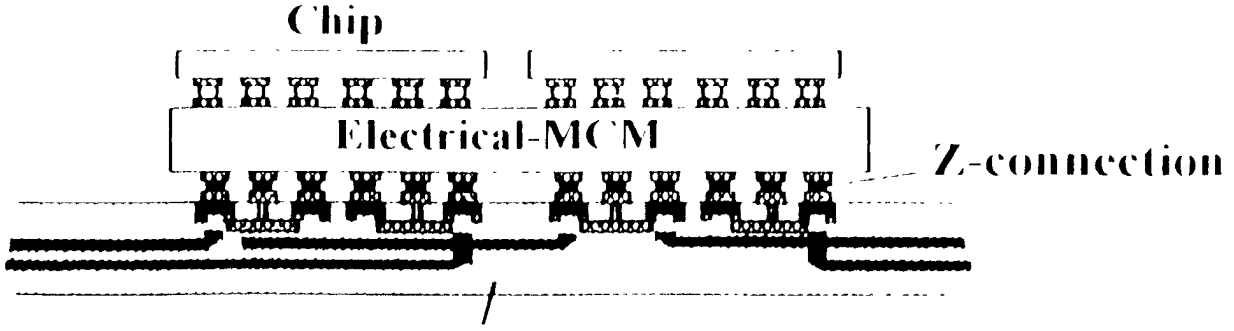
FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: OE-IP, OE-Film-MCM



F16.130





F16.131

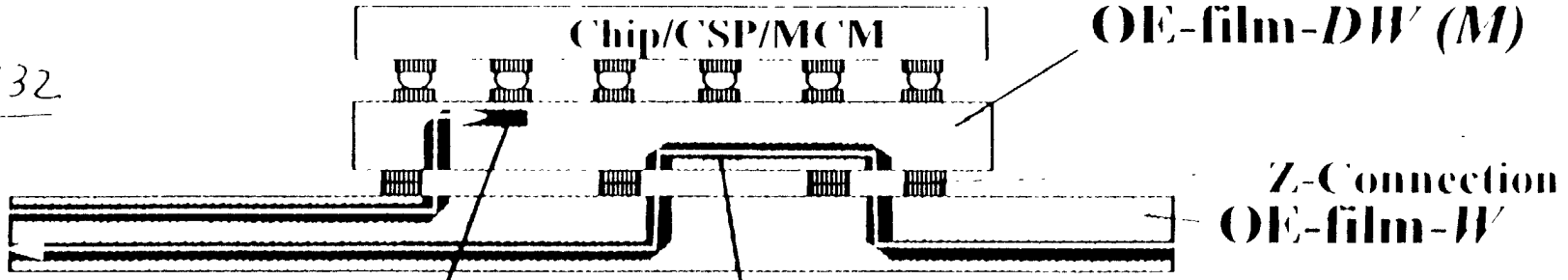
A15

(2/23/99) Fig. New-A1-Modified

A15 2/23/99 — (1 of 2)

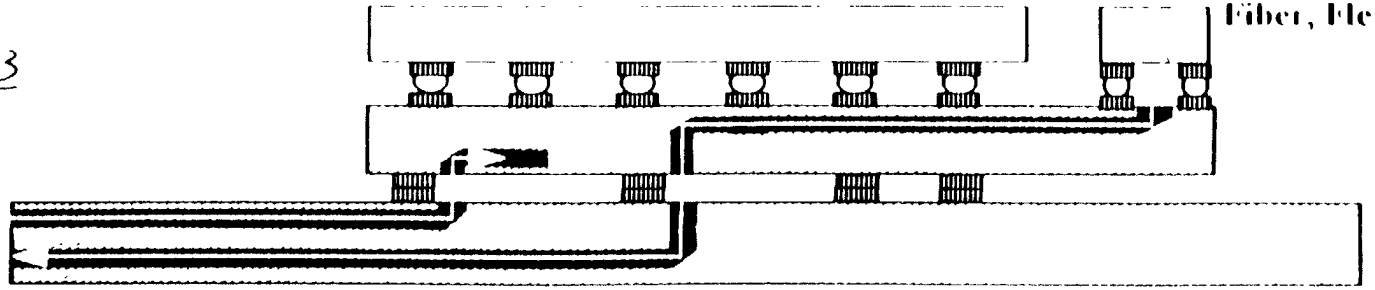
OE-film: Light Modulator Transmitters

Fig. 132



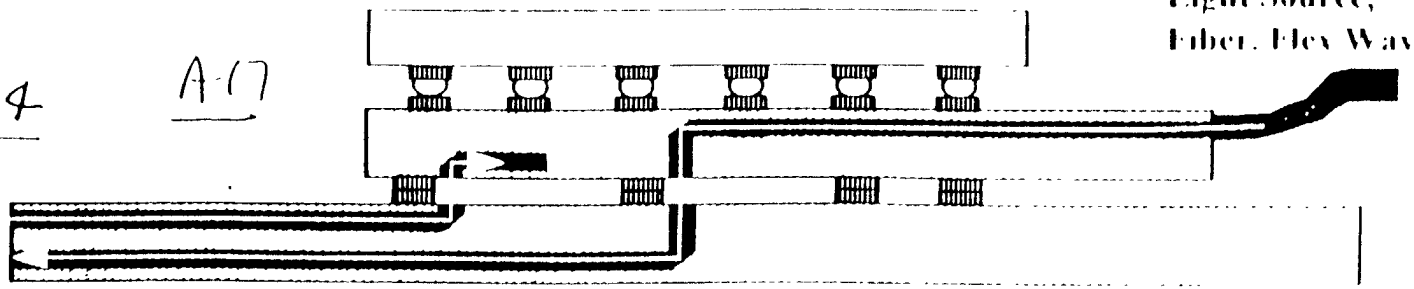
(2/17/99) Fig. A1(b-1)

Fig. 133



(2/17/99) Fig. A1(b-2)

Fig. 134 A-17

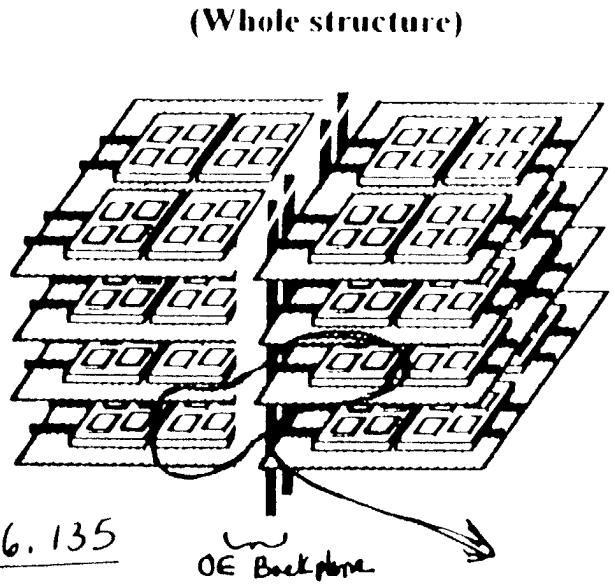


(2/23/99) Fig. A1(b-3)

Examples of Light Modulators: Electro-Optic (EO) Modulator, Electro-Absorption (EA) Modulator

FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: Both-Side Packaging



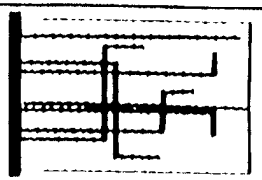
F16. 135

A 18

2/23/99-added 3'

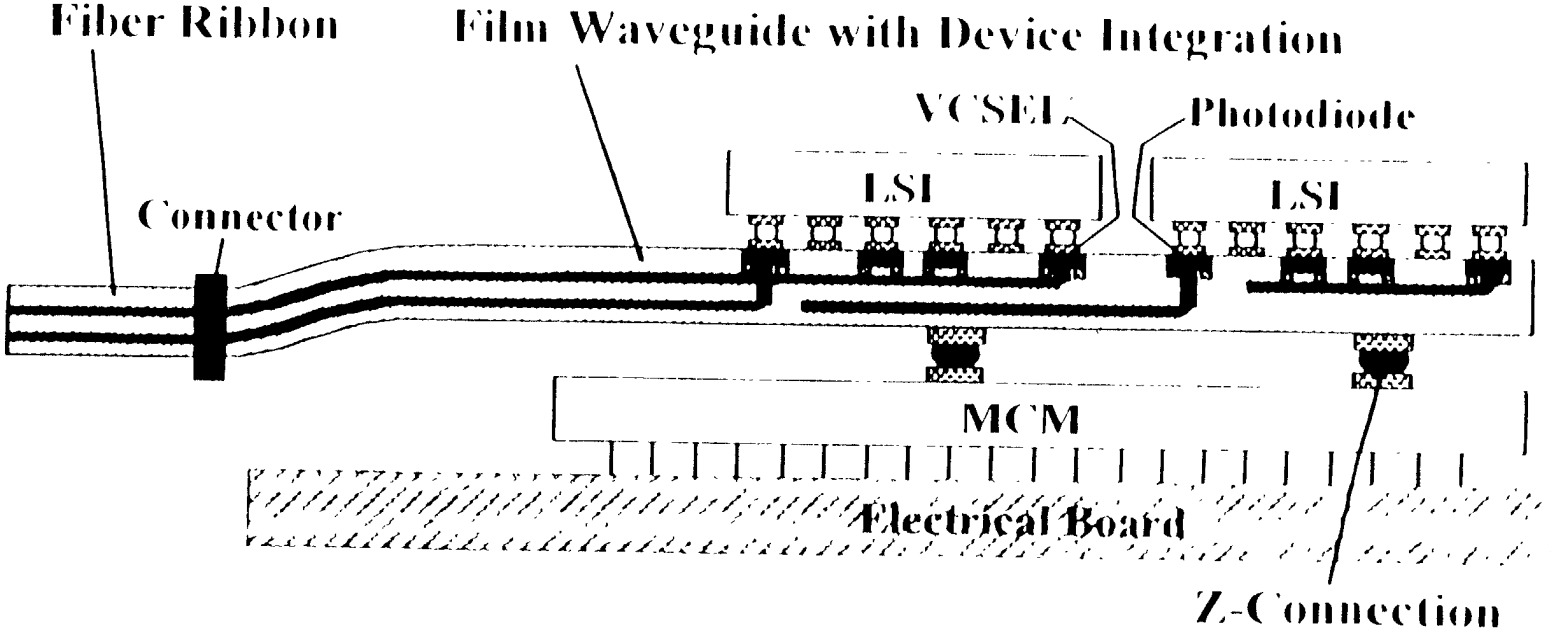
Figure 8

Direct Jump from LSI



Can act as
Line length cont

F16.136



F16.137

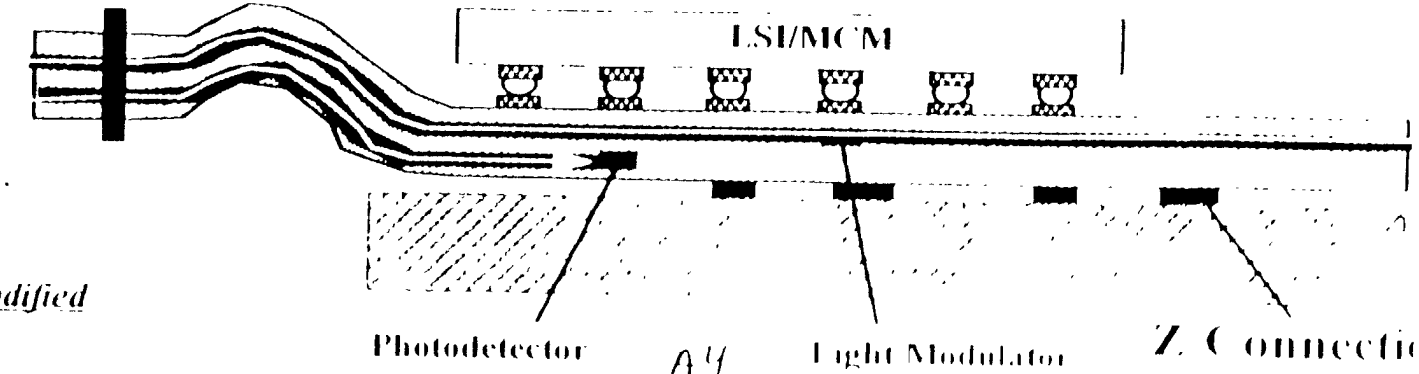
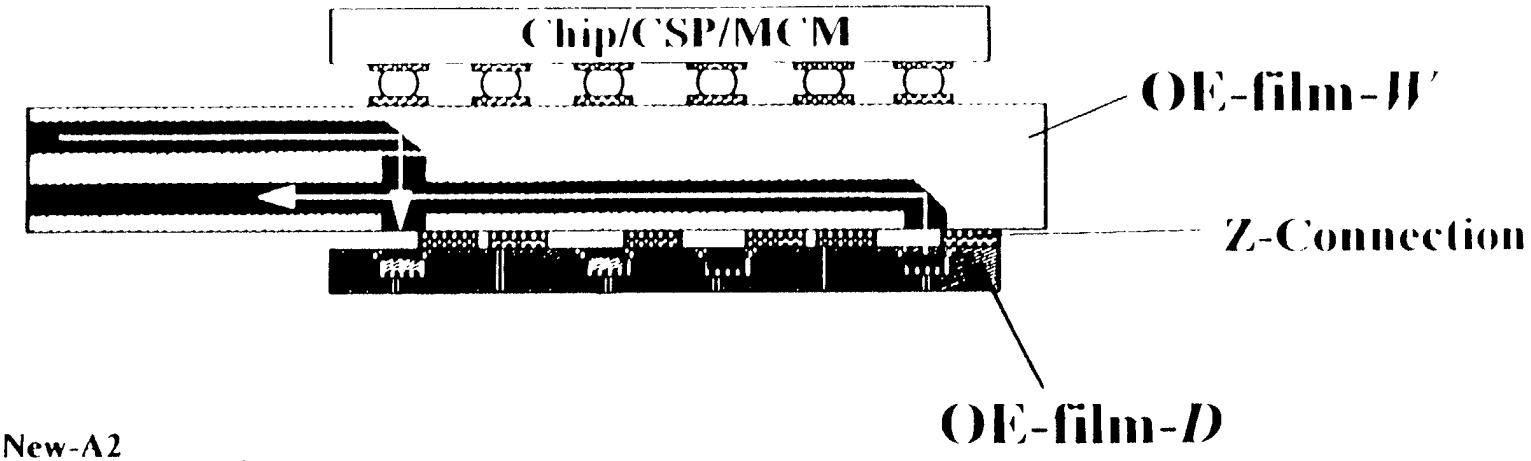


Fig. New-A4-Modified

A4

OE IP is Placed on the Oposit Side



(2/23/99) Fig. New-A2

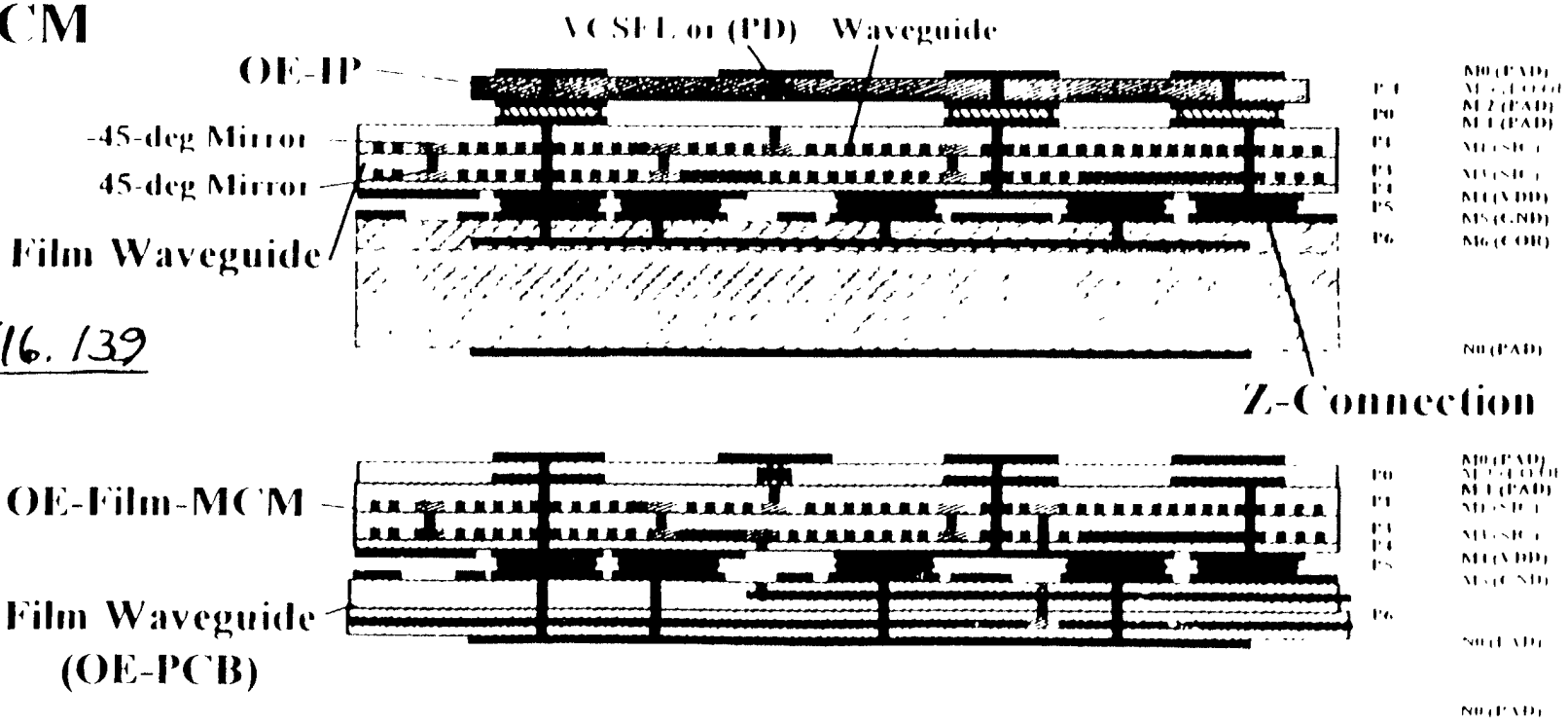
F16.13B

A20

OE MCM

OE-MCM

GS
MPS
PC



F16. 139

F16. 140

A5

Fig. A5-Modified

A5 1/18/99

FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: Smart Pixel

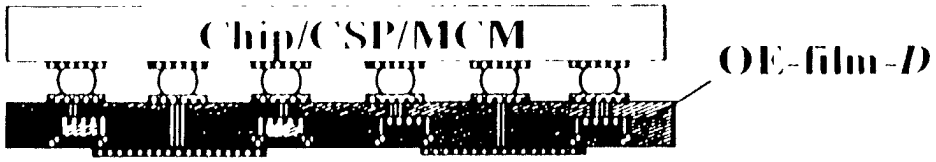
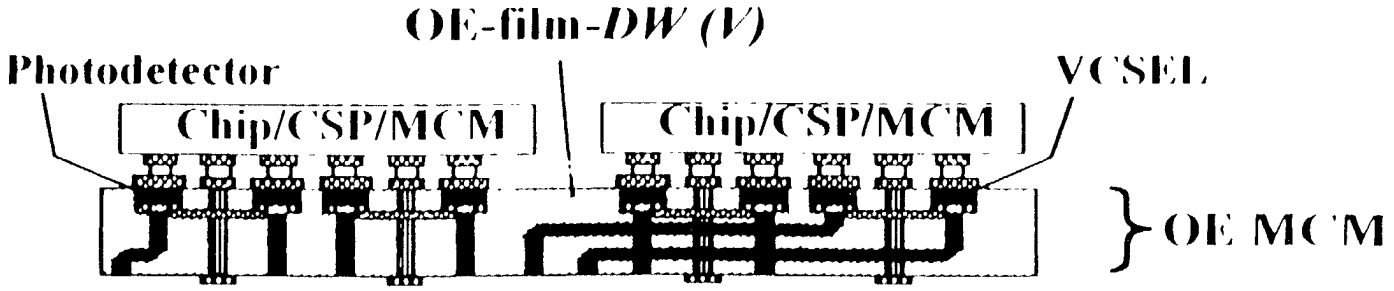


FIG 141

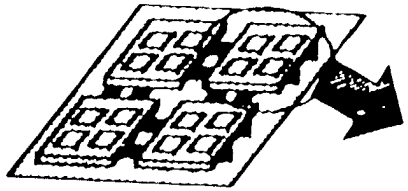


A16

FIG. 142

2/23/99-added 6'

OE-Film/OE-Film Stack --- Back-Side Connection



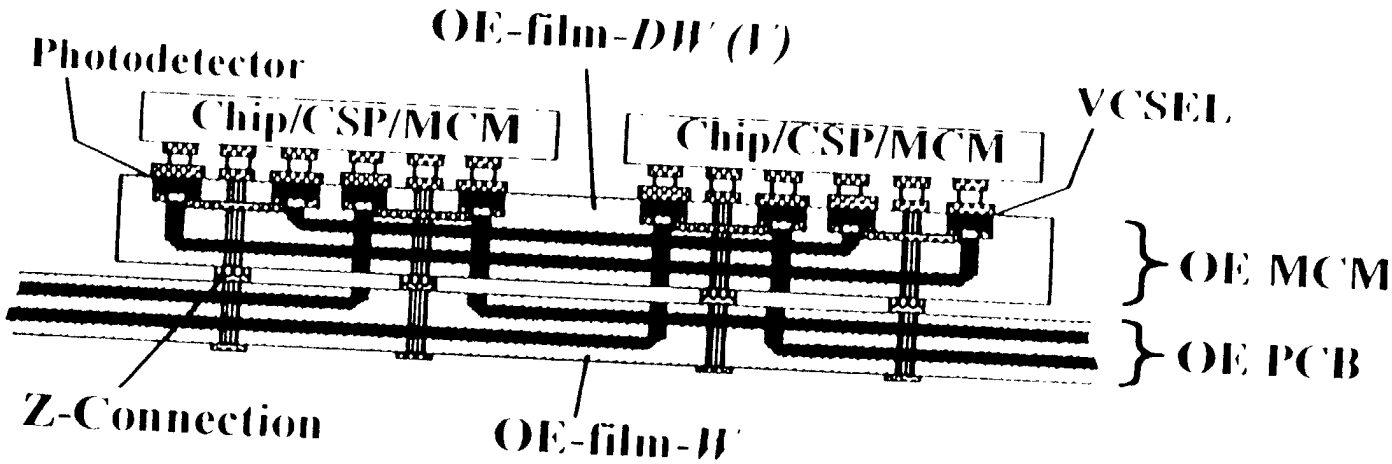


FIG. 14B

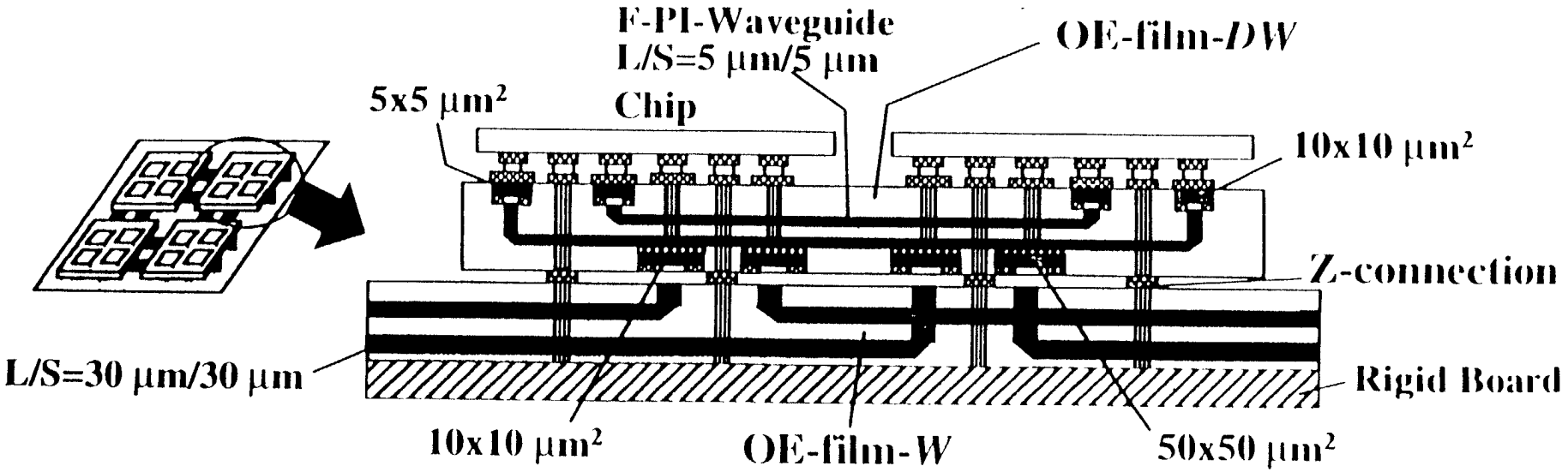
A19

2/23/99-added 4'

Figure 9

A19 2/7/00

OE-Film/OE-Film Stack --- Back-Side Connection



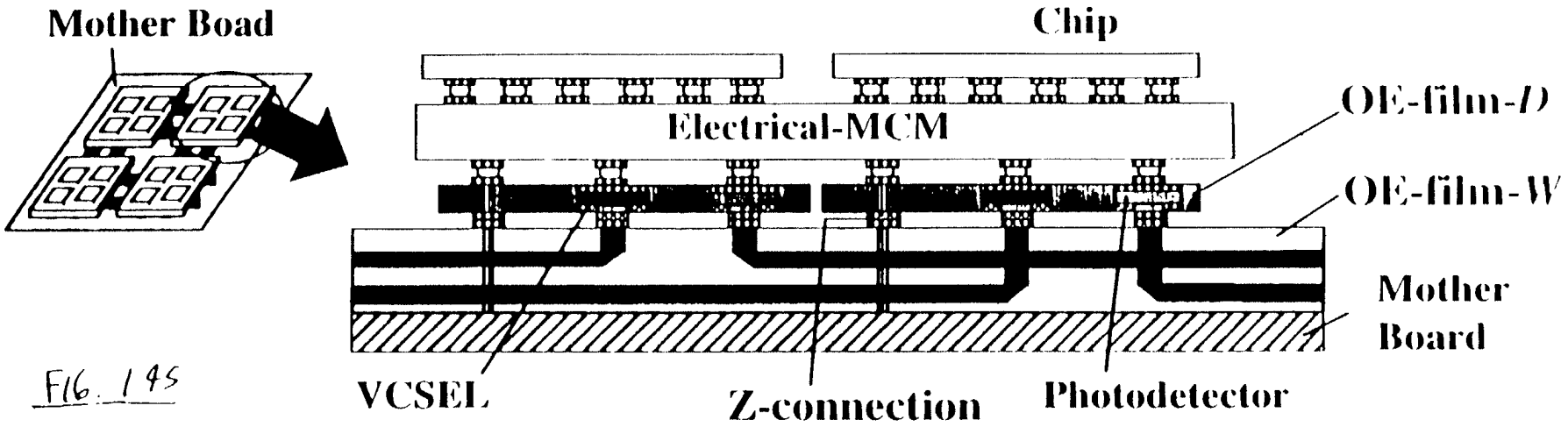
D1

Fig. 3/18/99-1

D1 3/18/99

FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-MCM/OE-Bord Stack



F16. 14S

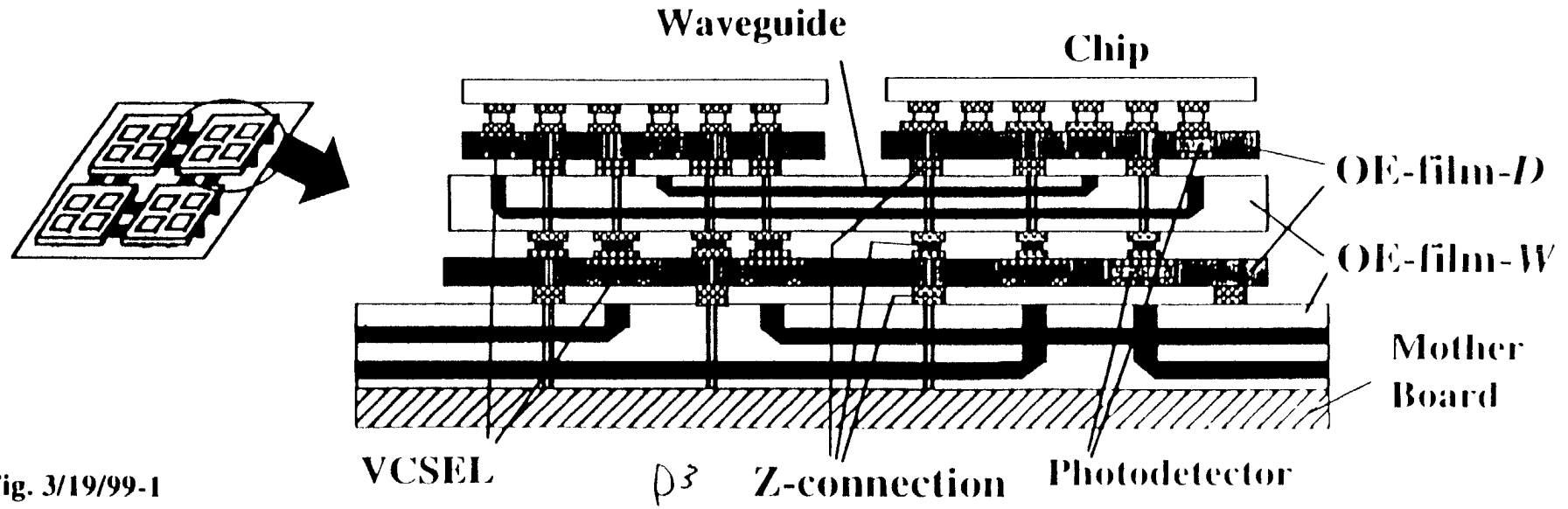
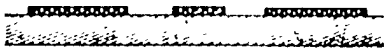


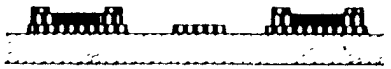
Fig. 3/19/99-1

F16. 14b

D3 3/18/99

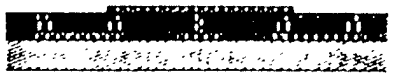
Device Integration Process

(1) Pads/Lines formation  FIG. 14J

(2) Placement of Thin film devices  FIG. 14B

(3) Polymer coat  FIG 14J

(4) Planarization  FIG 13J

(5) Vias/Pads/Lines formation  FIG 15J

(6) Substrate removal  FIG 18J

OE-film-*D*

A 21

(6') Jump to the waveguide formation process

 FIG 16J

OE-film-*DW(T)*

2/17/99-added 5

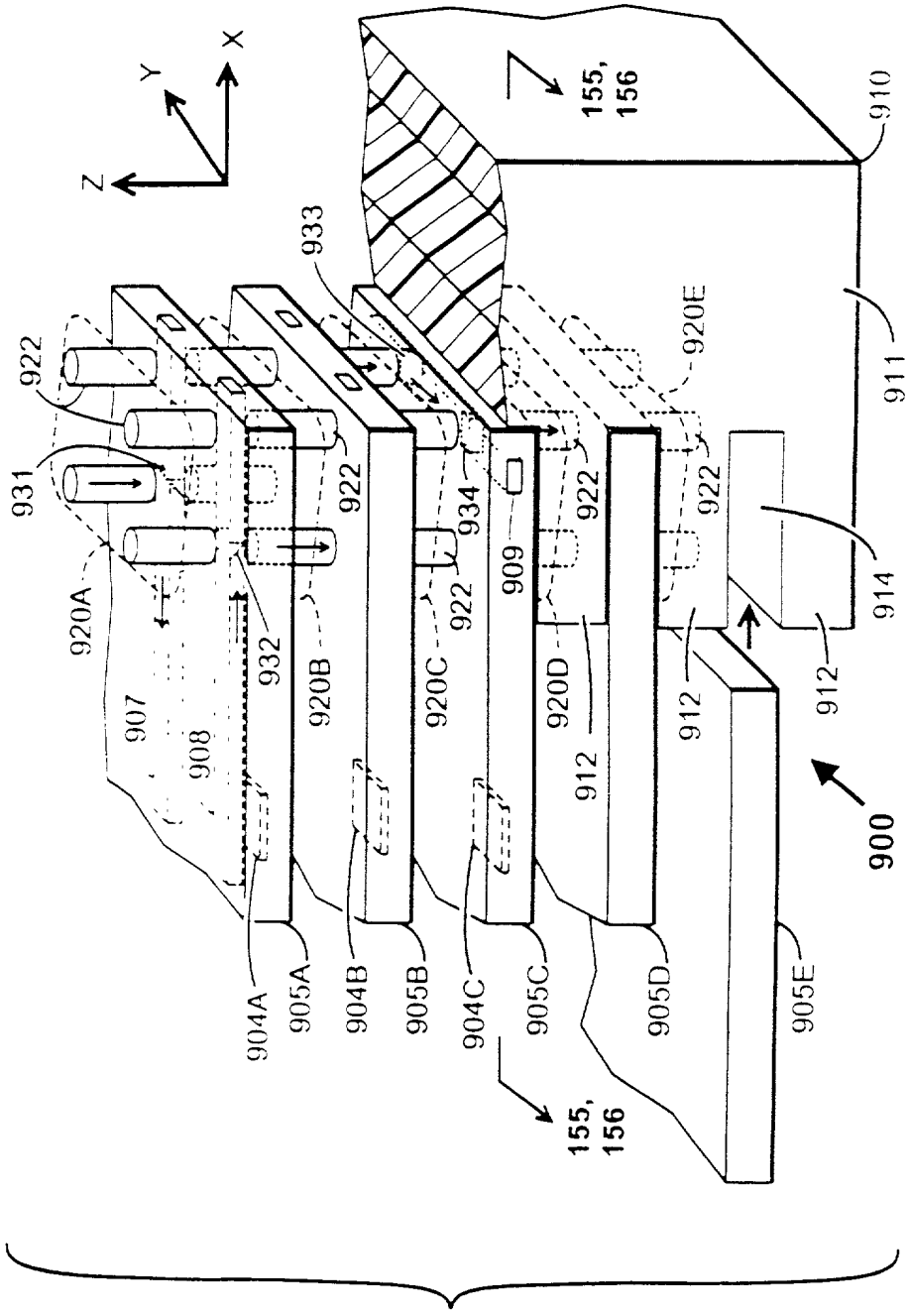

Z
Y
X
155, 156
910
933
922
931
911
920E
920A
907
908
932
920B
920C
922
934
909
920D
912
914
900
904A
905A
904B
905B
904C
905C
905D
905E

FIG._154

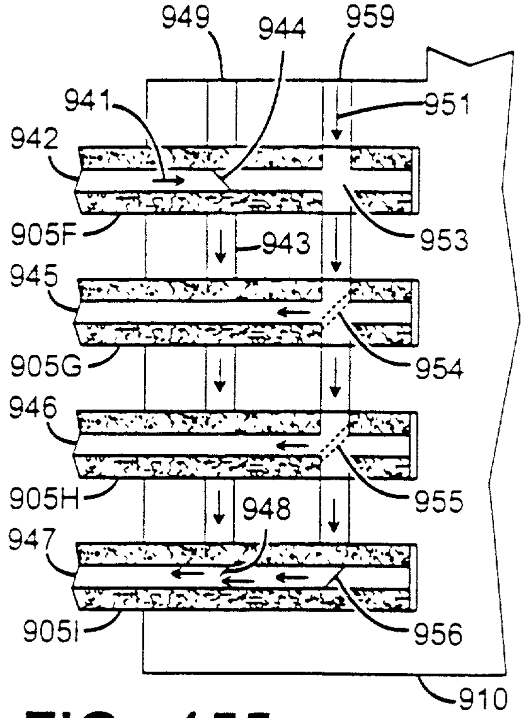


FIG._155

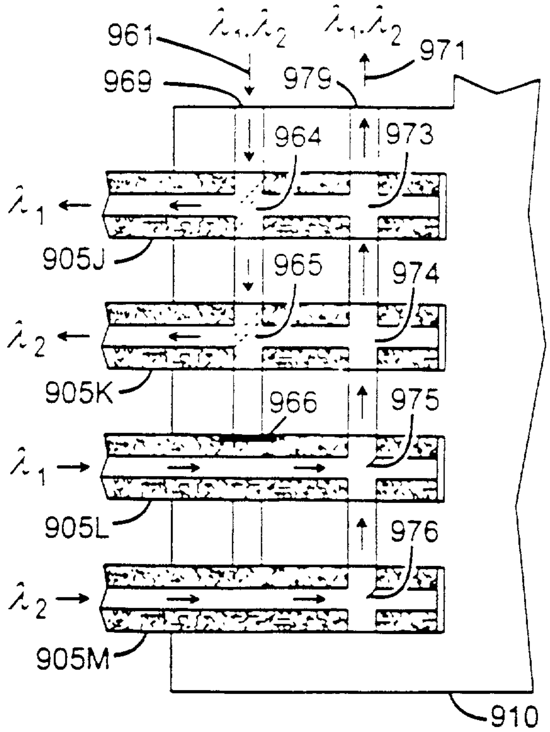


FIG._156-1

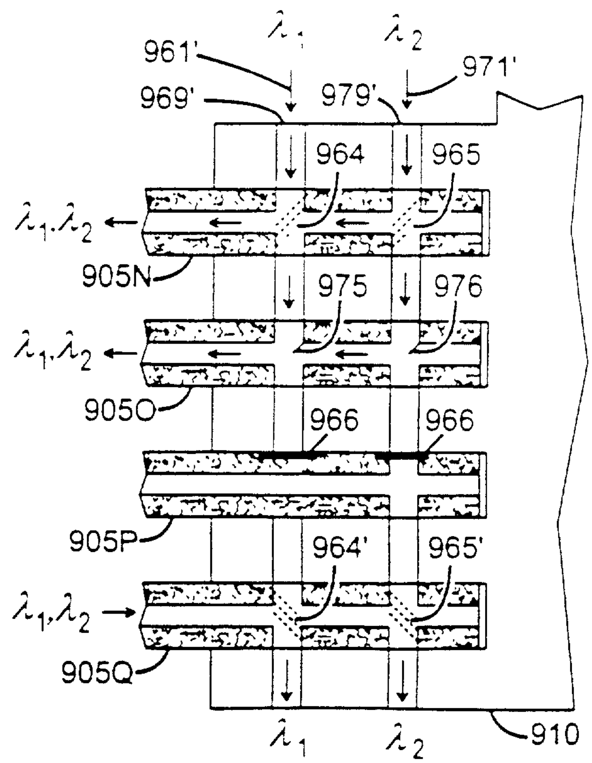


FIG._156-2

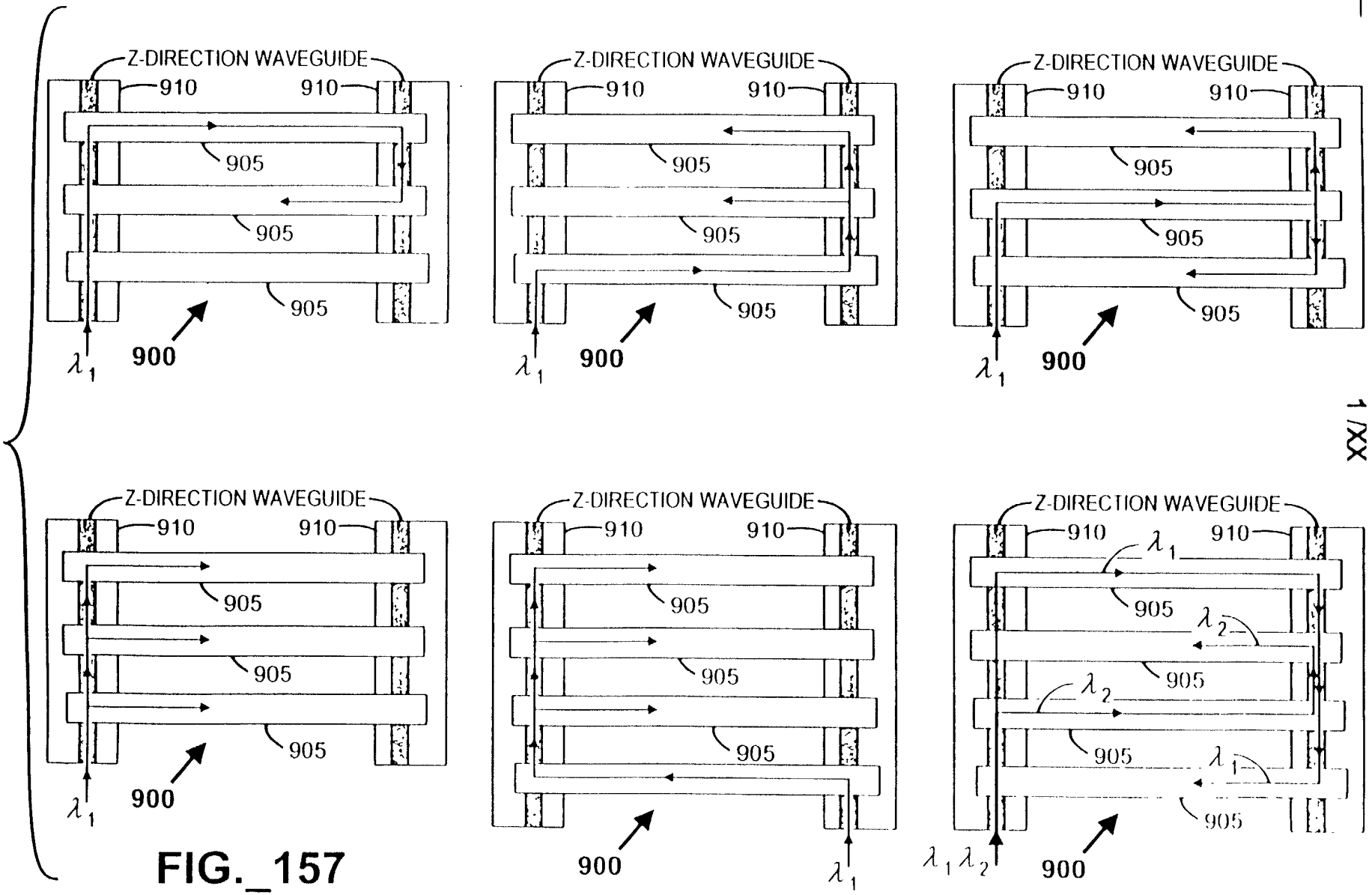


FIG._157

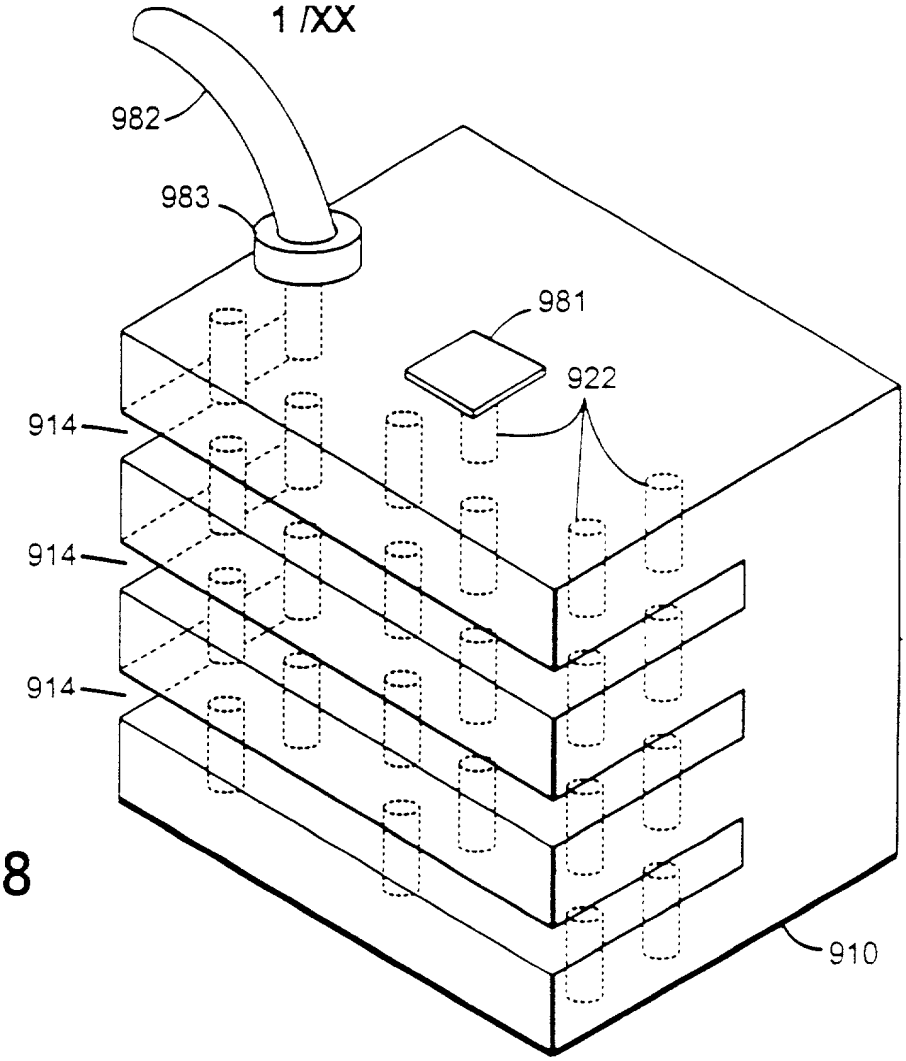


FIG._158

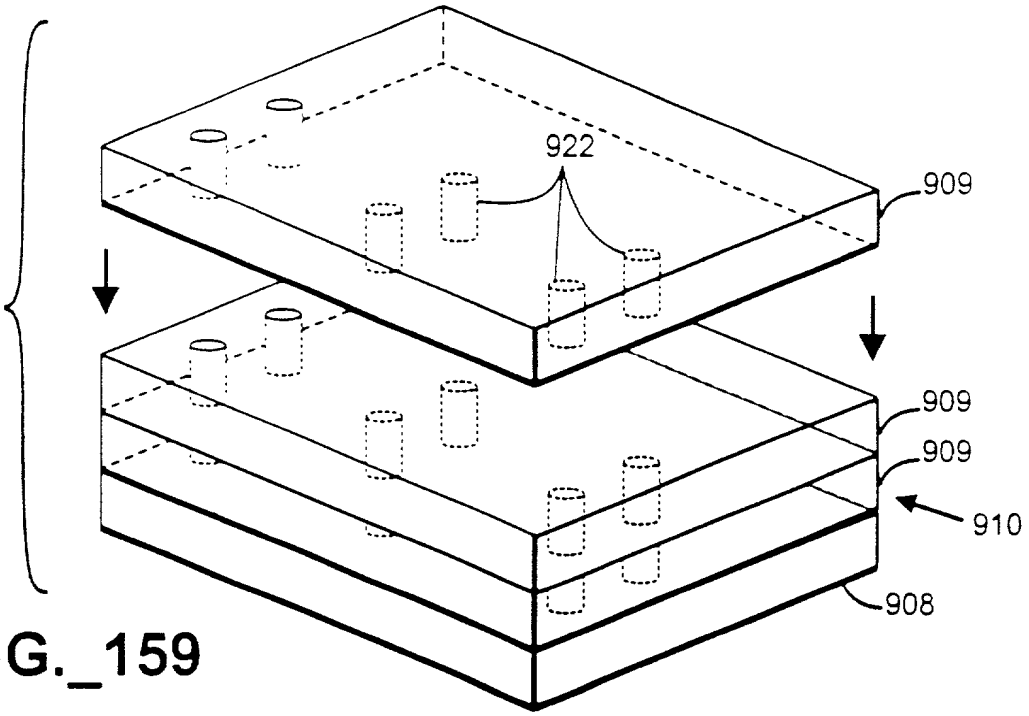


FIG._159

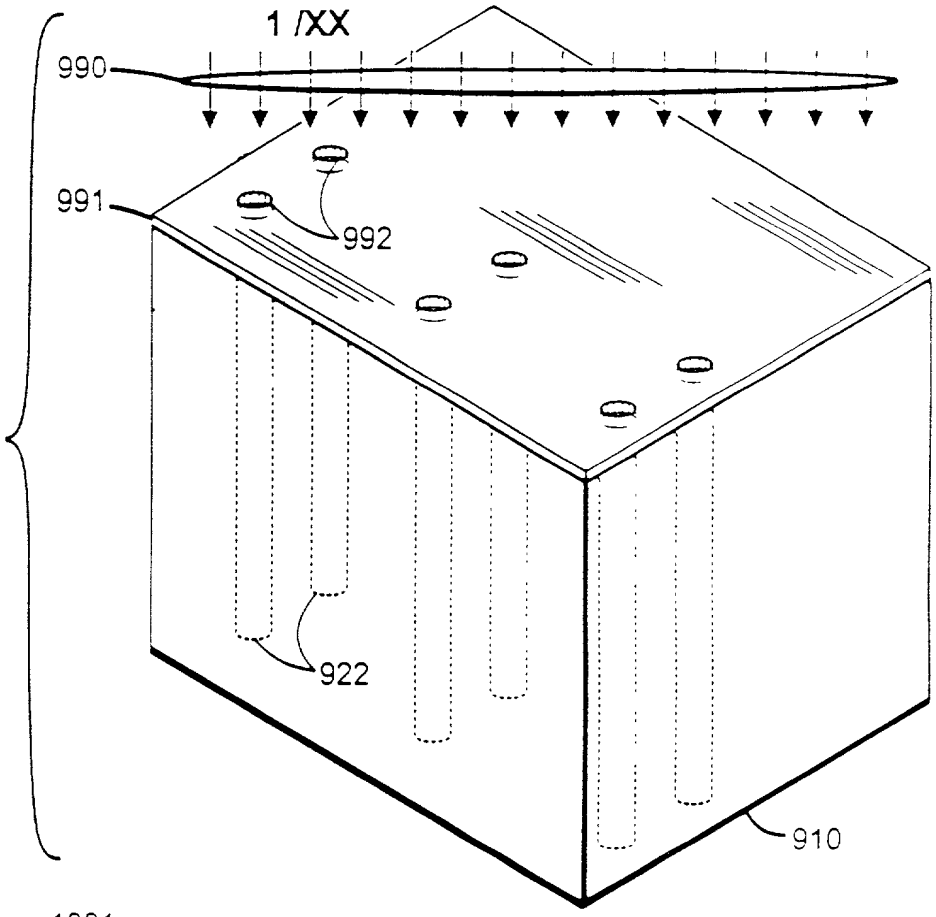


FIG._160

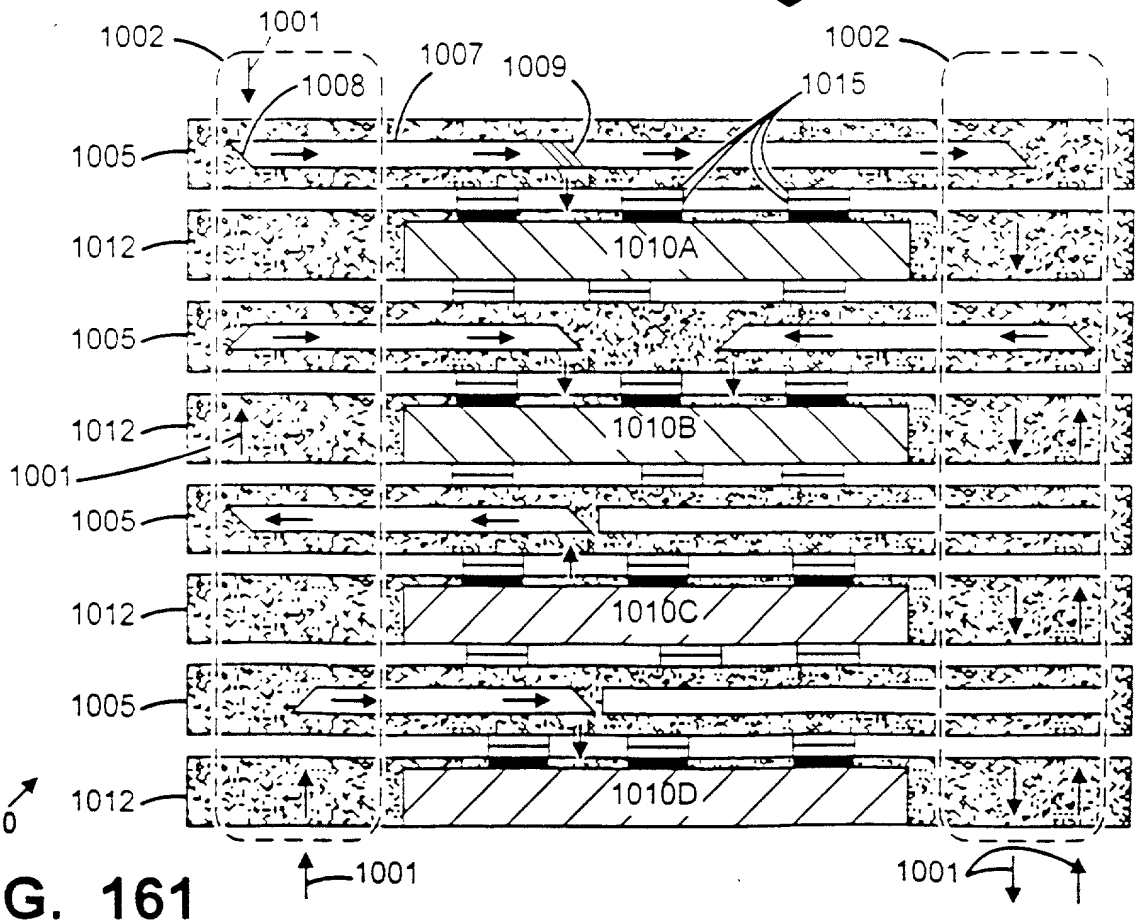


FIG._161

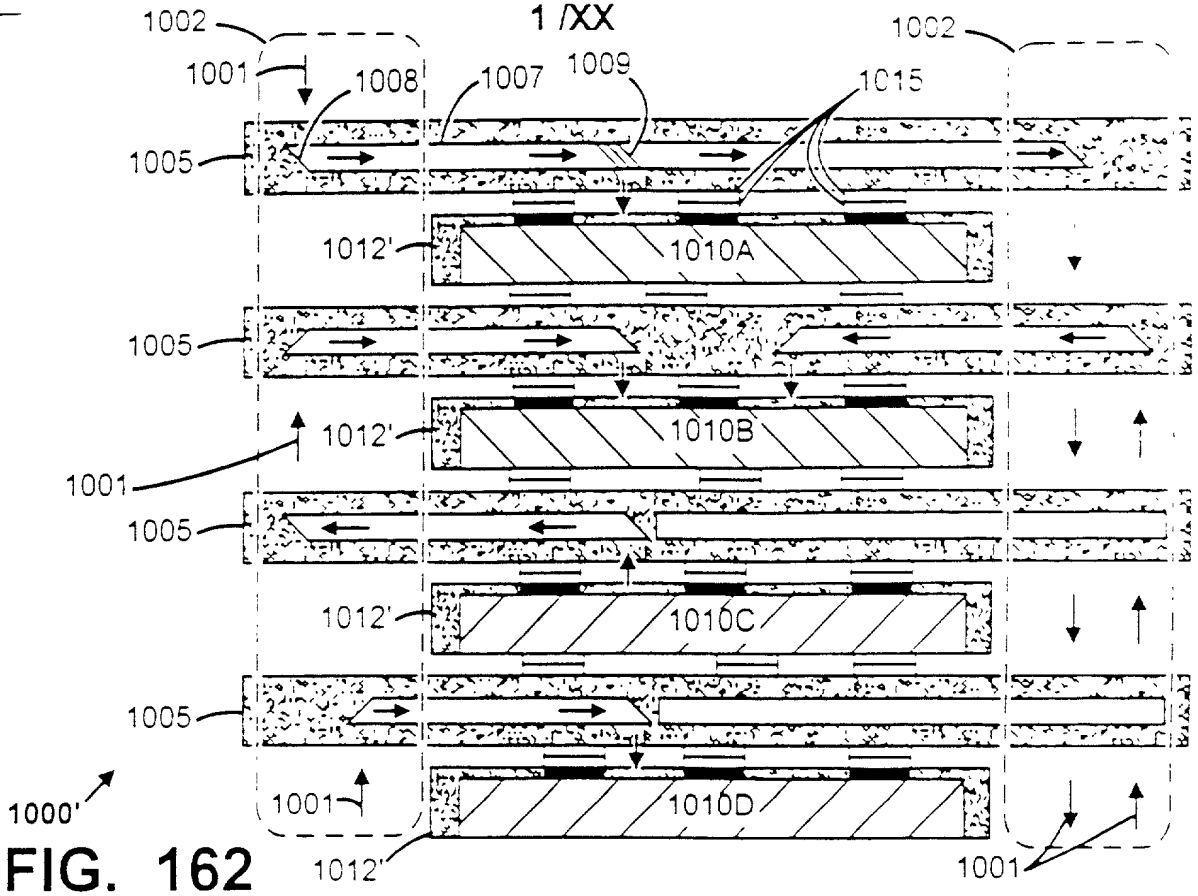


FIG._162

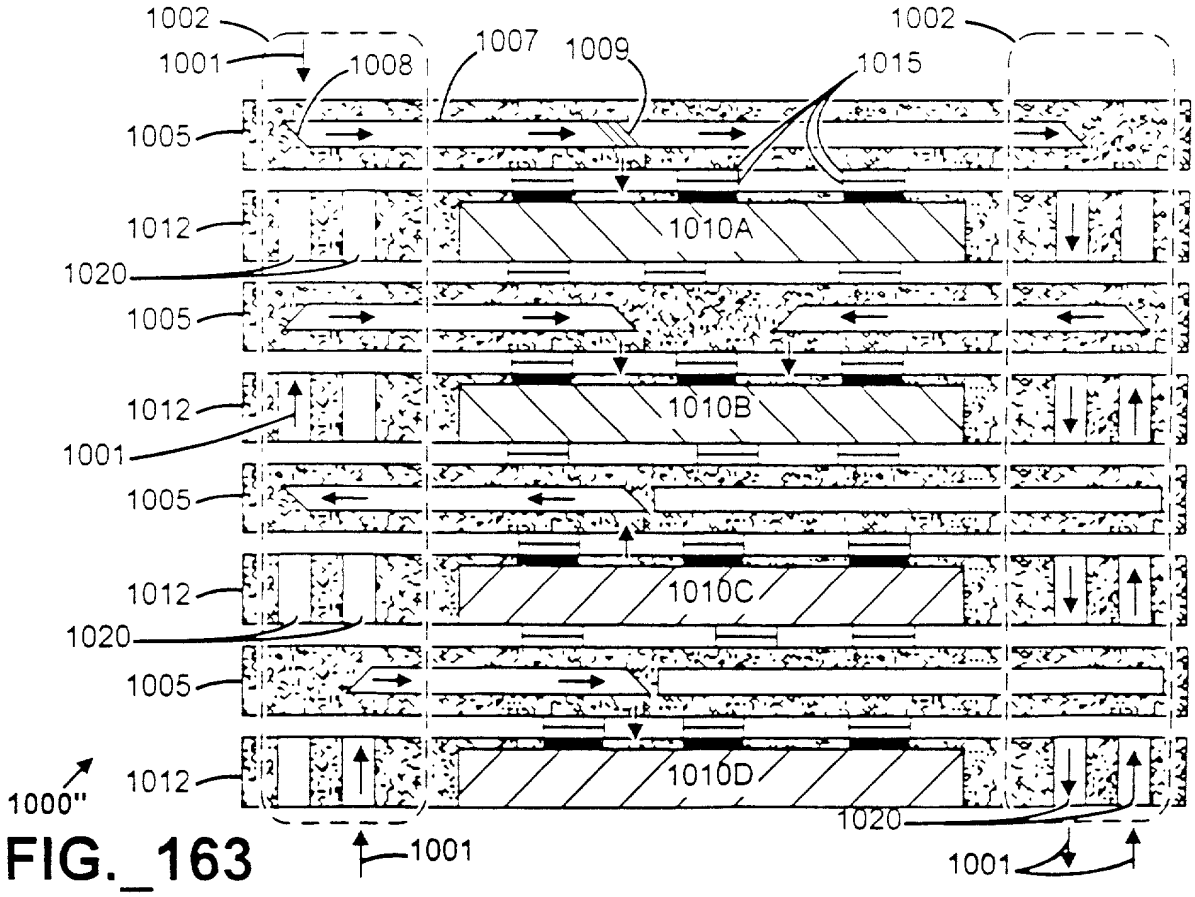


FIG._163

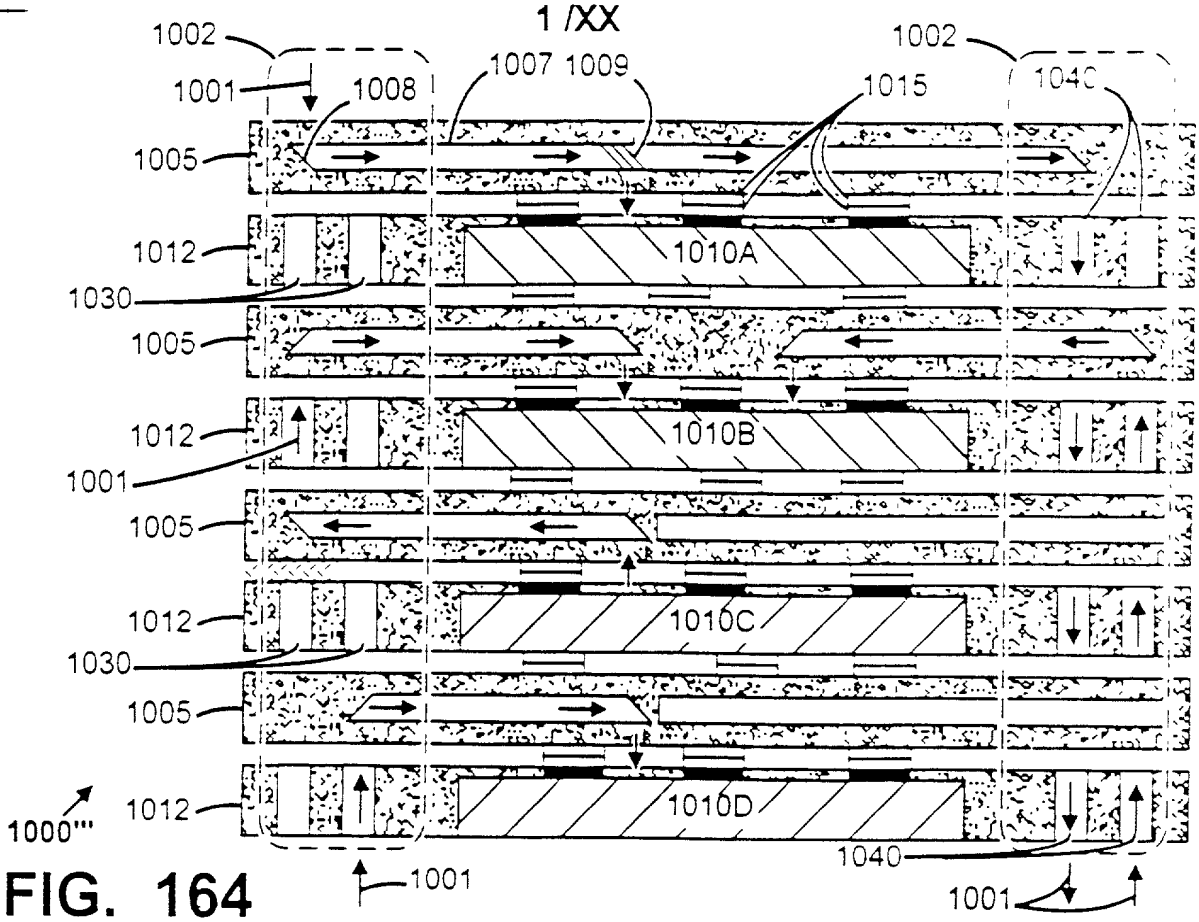


FIG._164

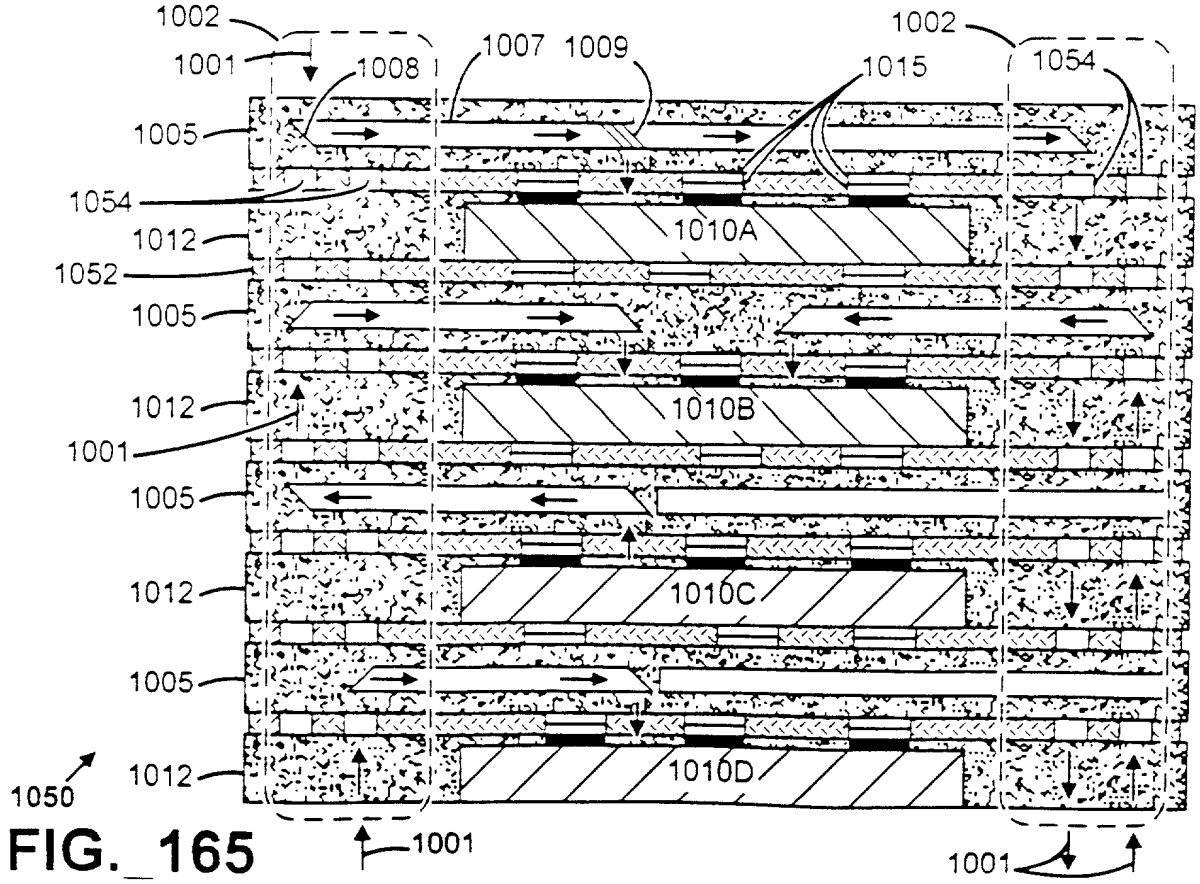


FIG._165

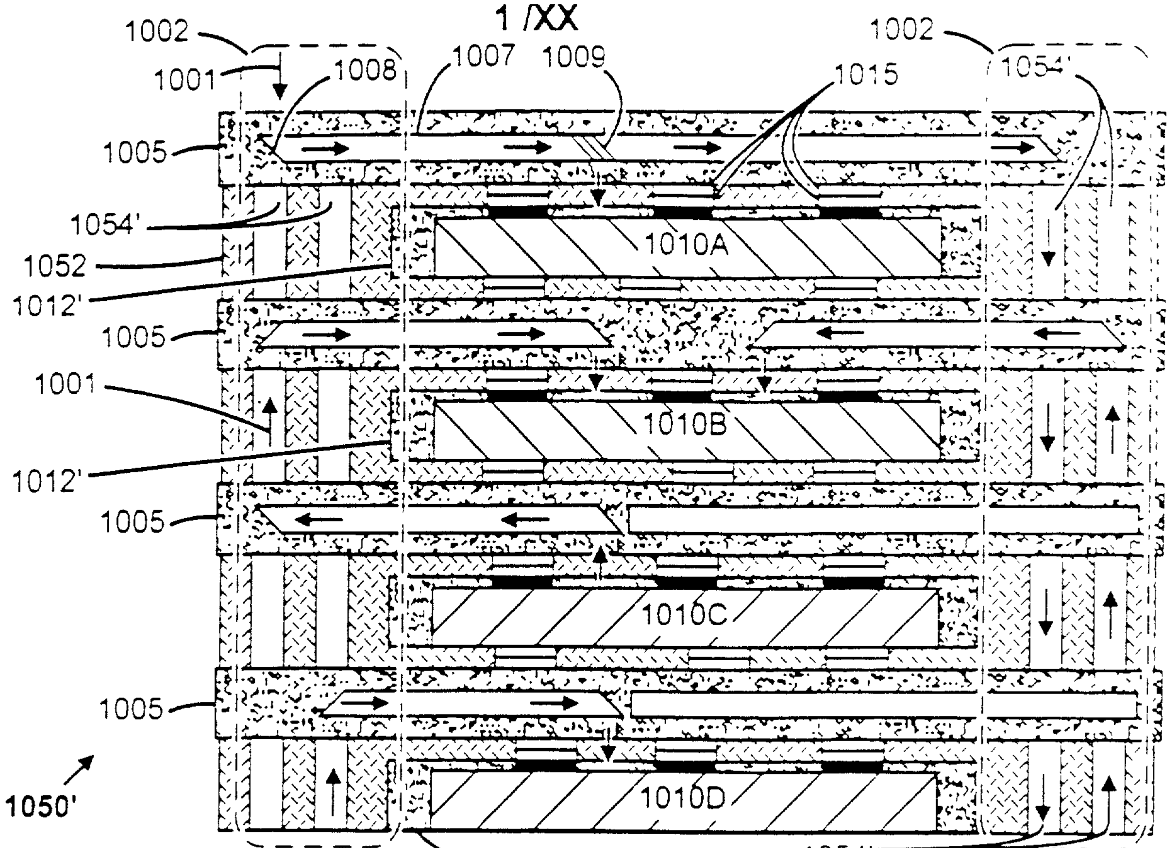


FIG._166

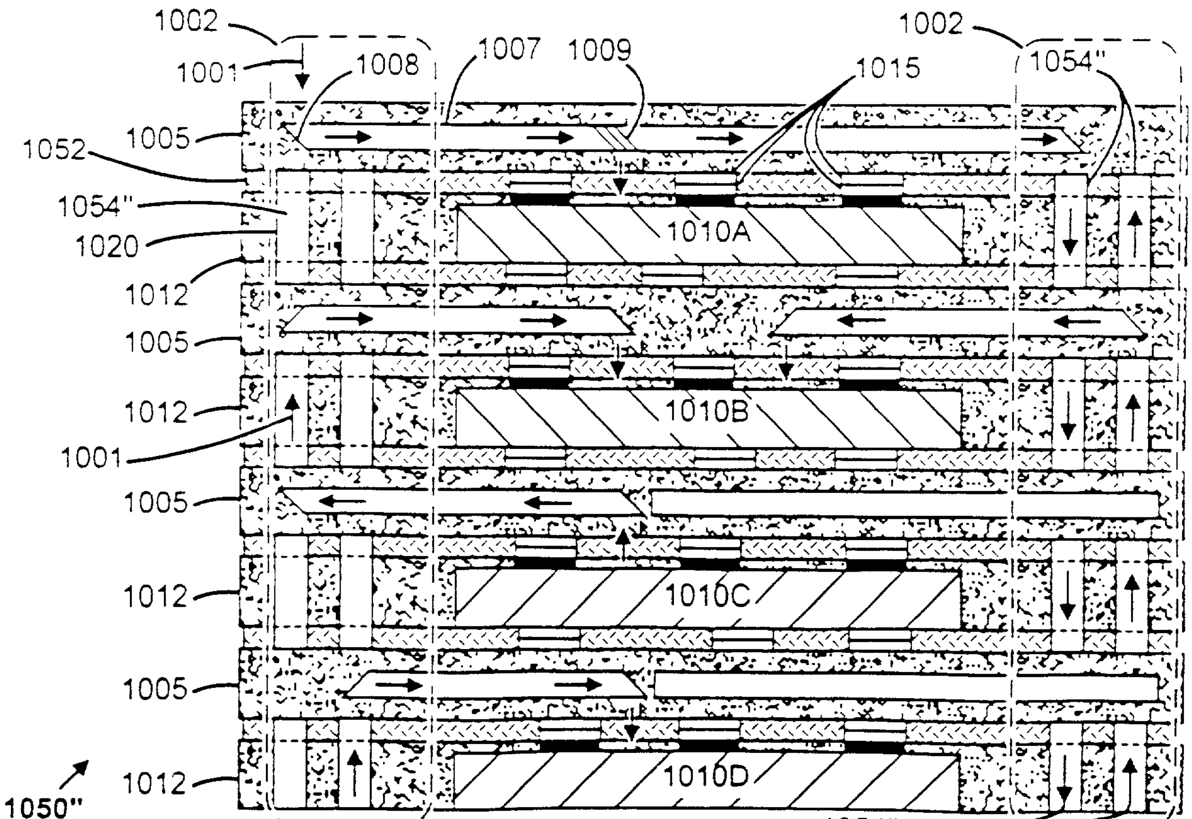


FIG._167

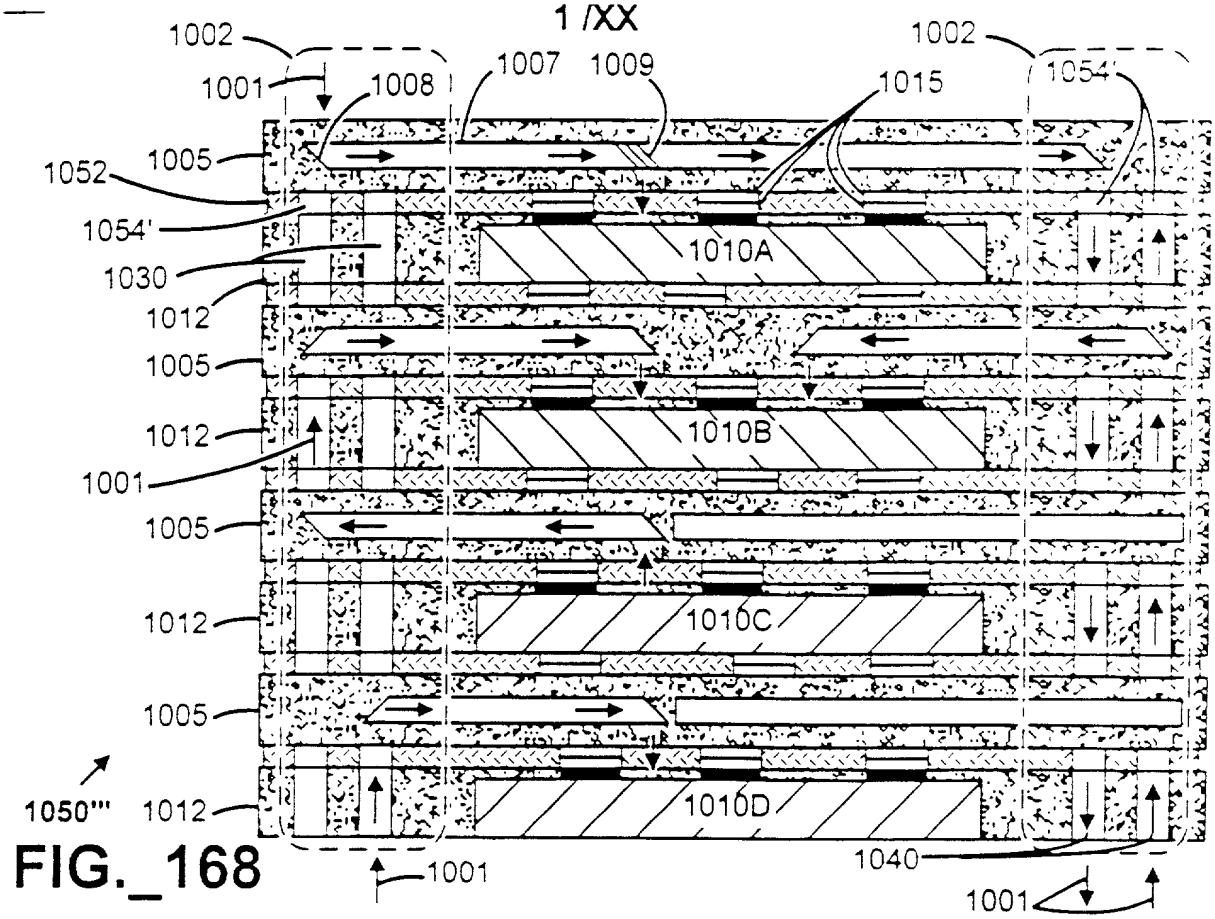


FIG._168

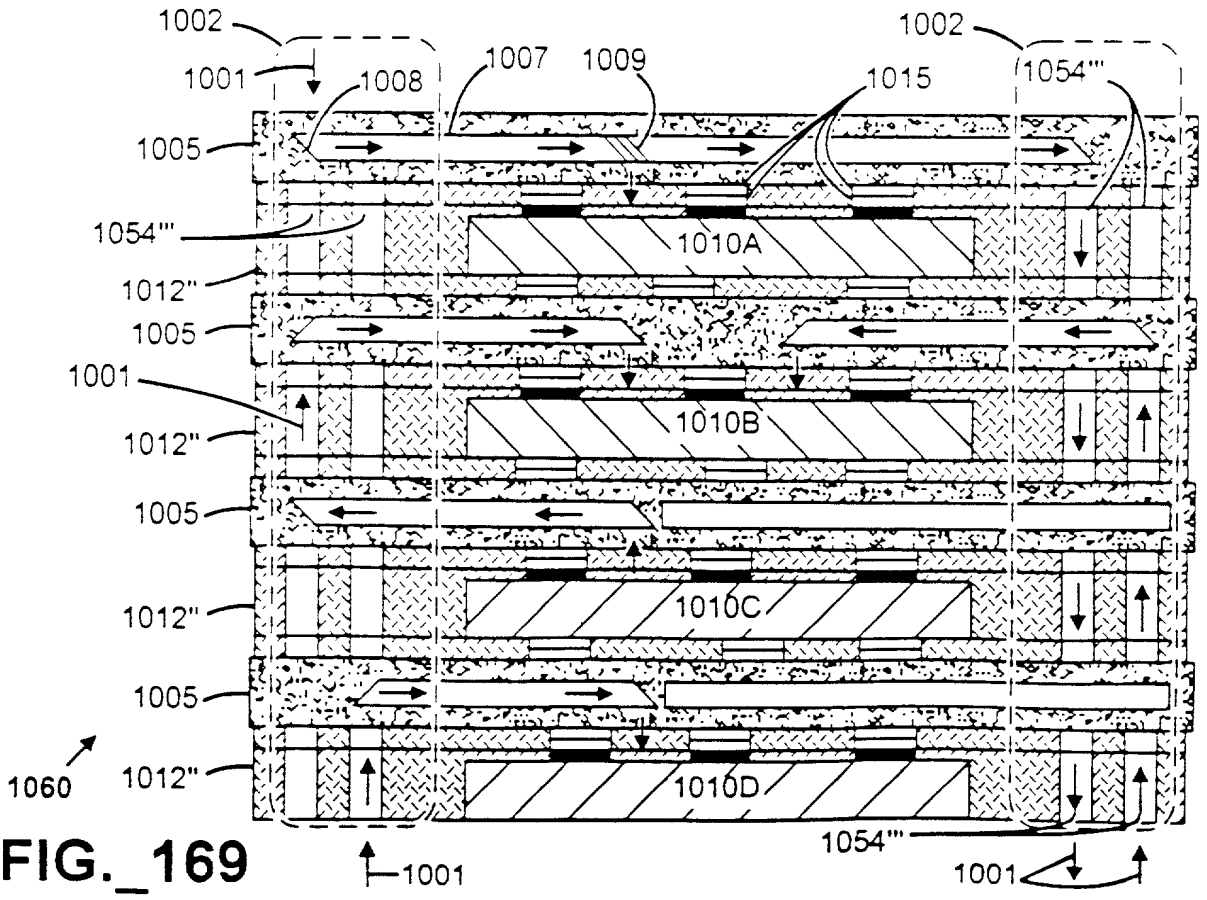


FIG._169

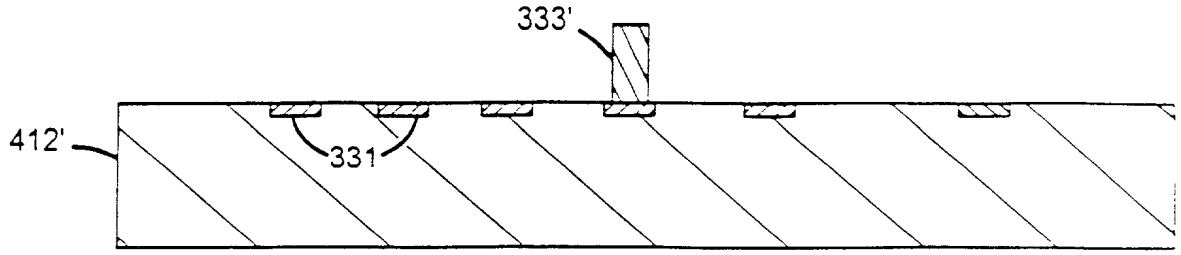


FIG._170

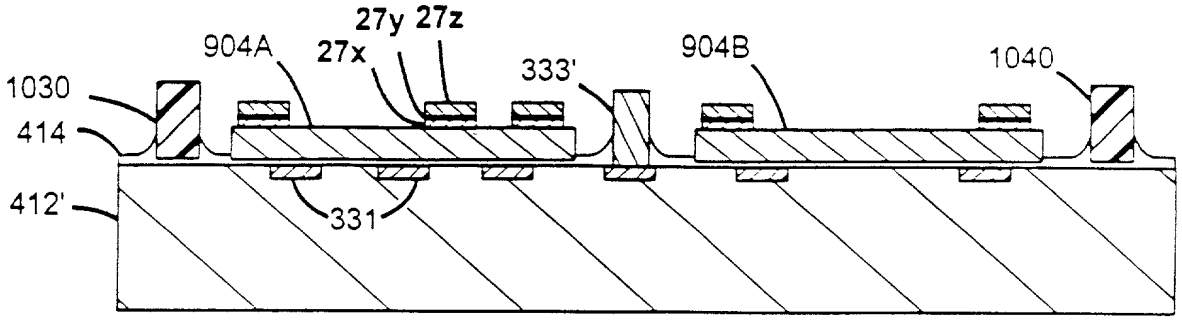


FIG._171

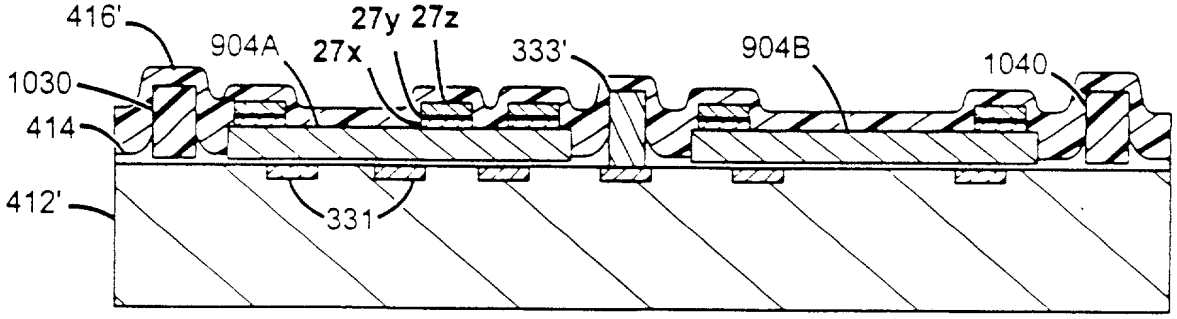


FIG._172

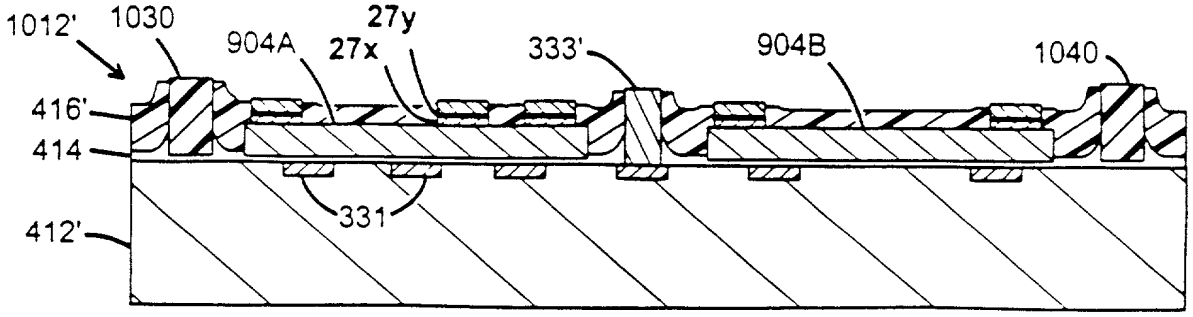


FIG._173

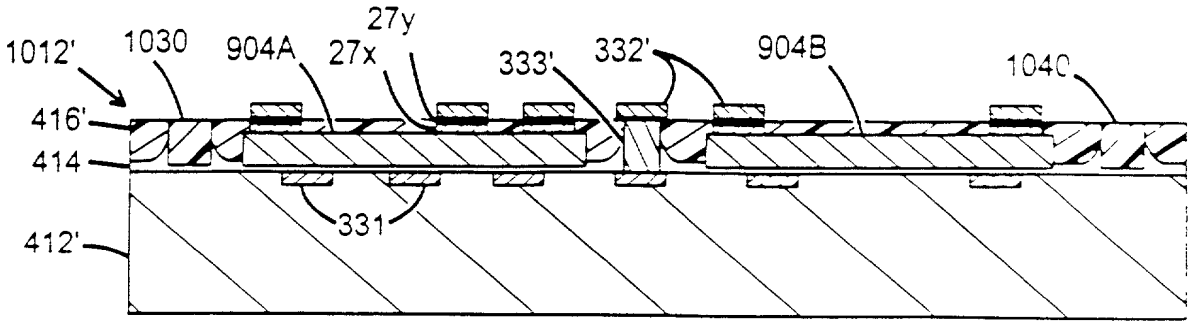


FIG._174

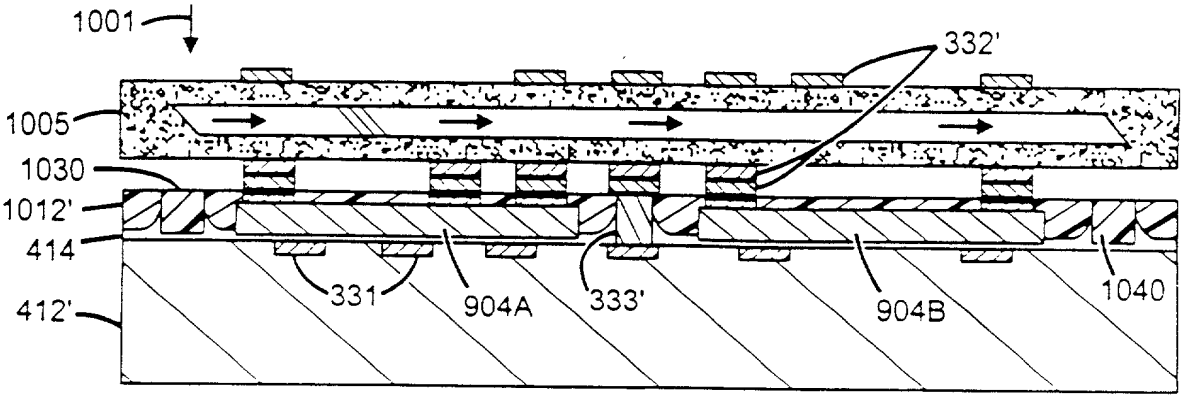


FIG._175

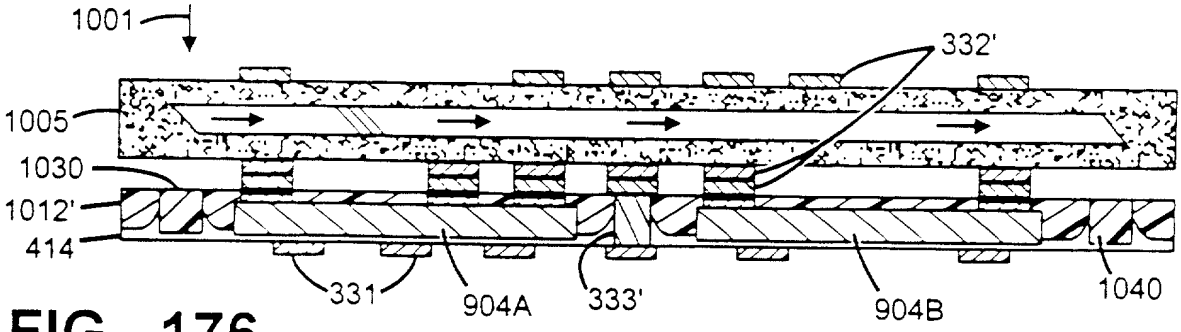


FIG._176

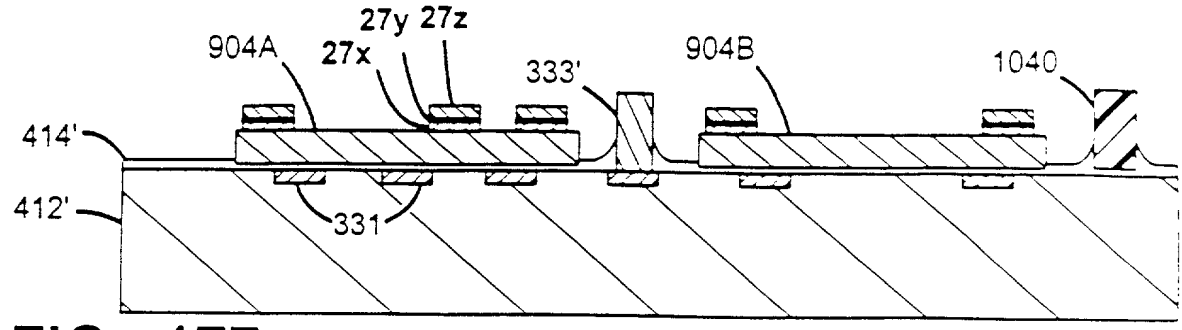


FIG._177

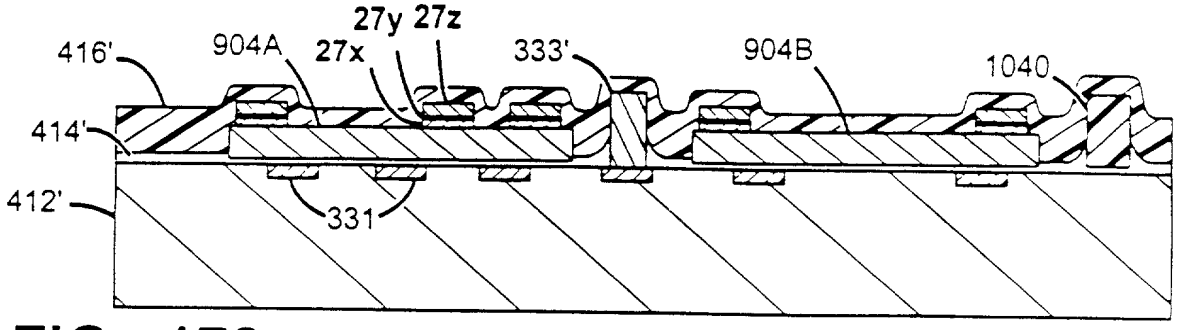


FIG._178

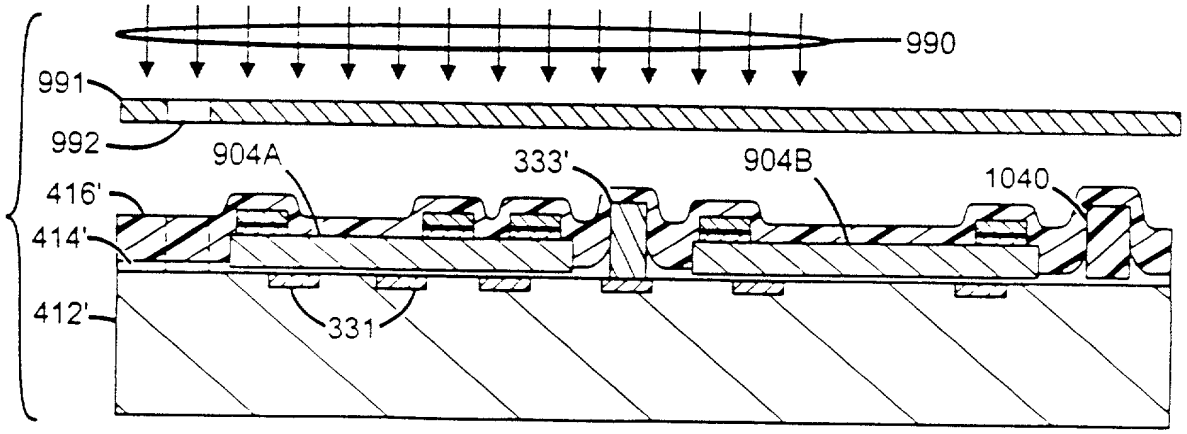


FIG._179

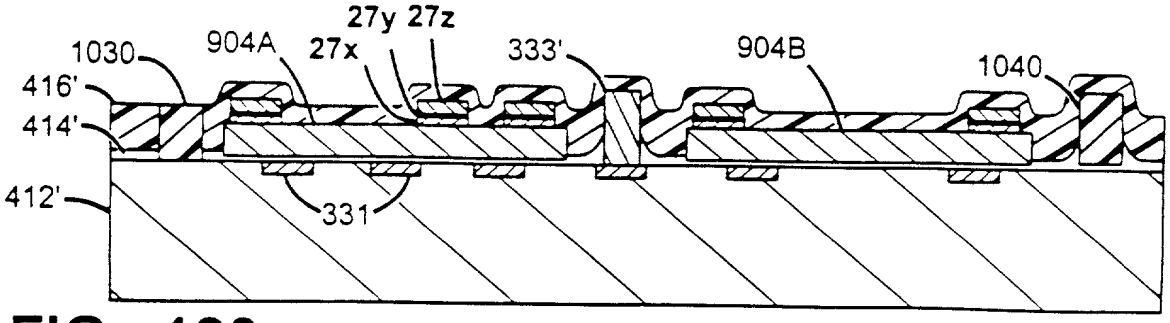


FIG._180

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Planar Modulator)

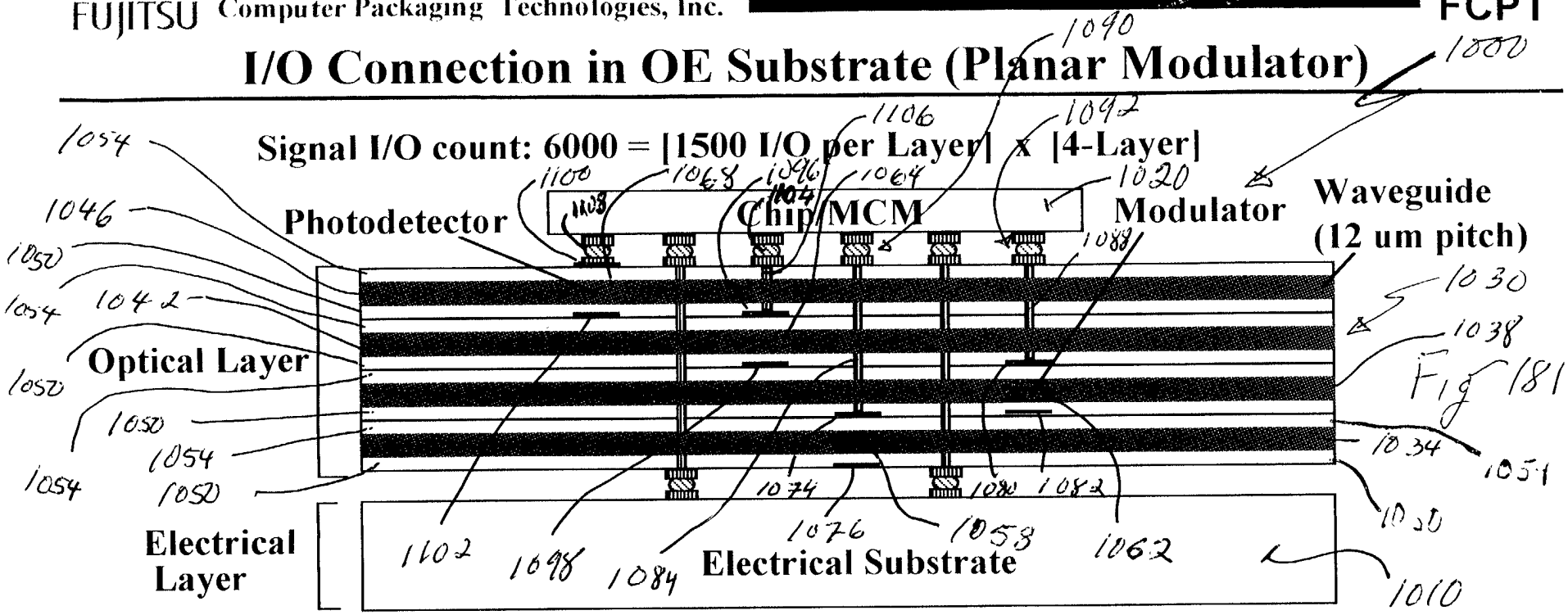


Fig 181

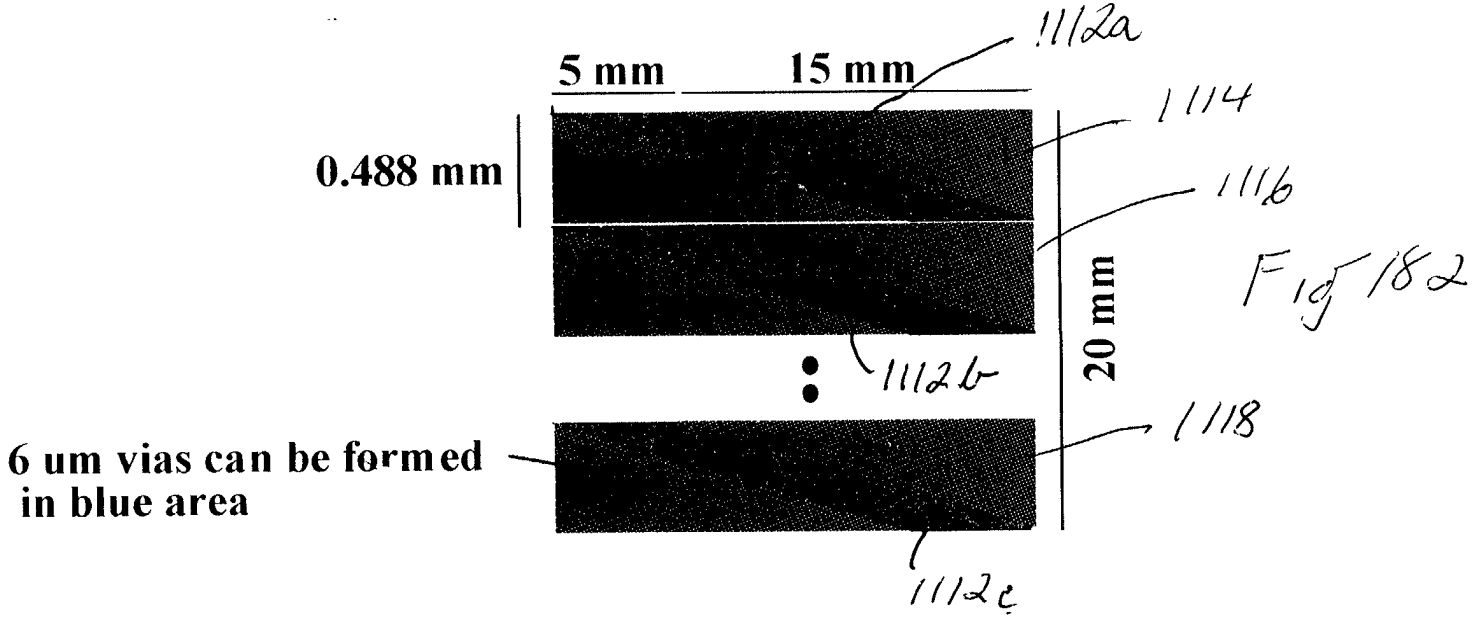
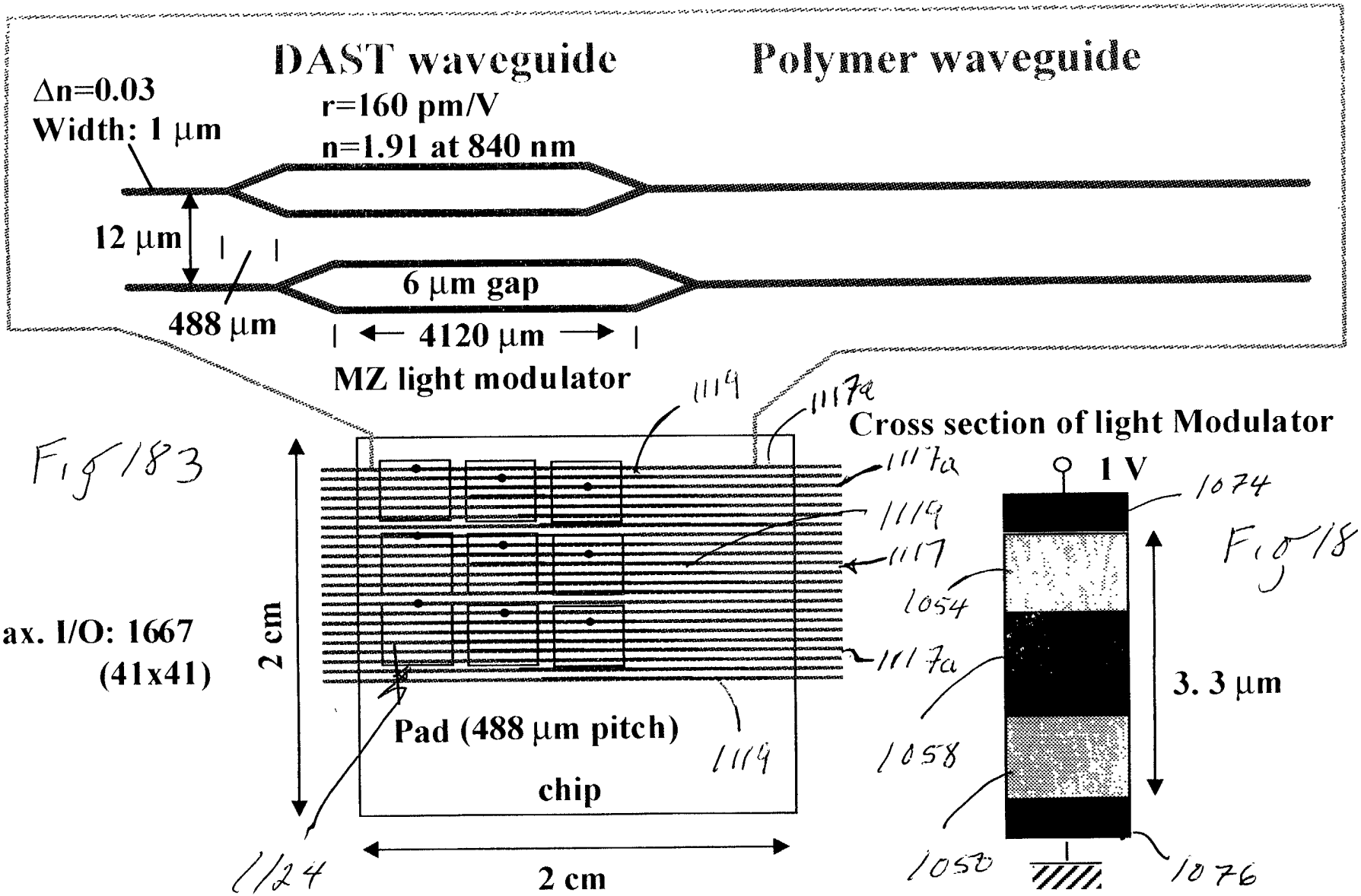


Fig 182

I/O Connection in OE Substrate (Planar Modulator)



FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

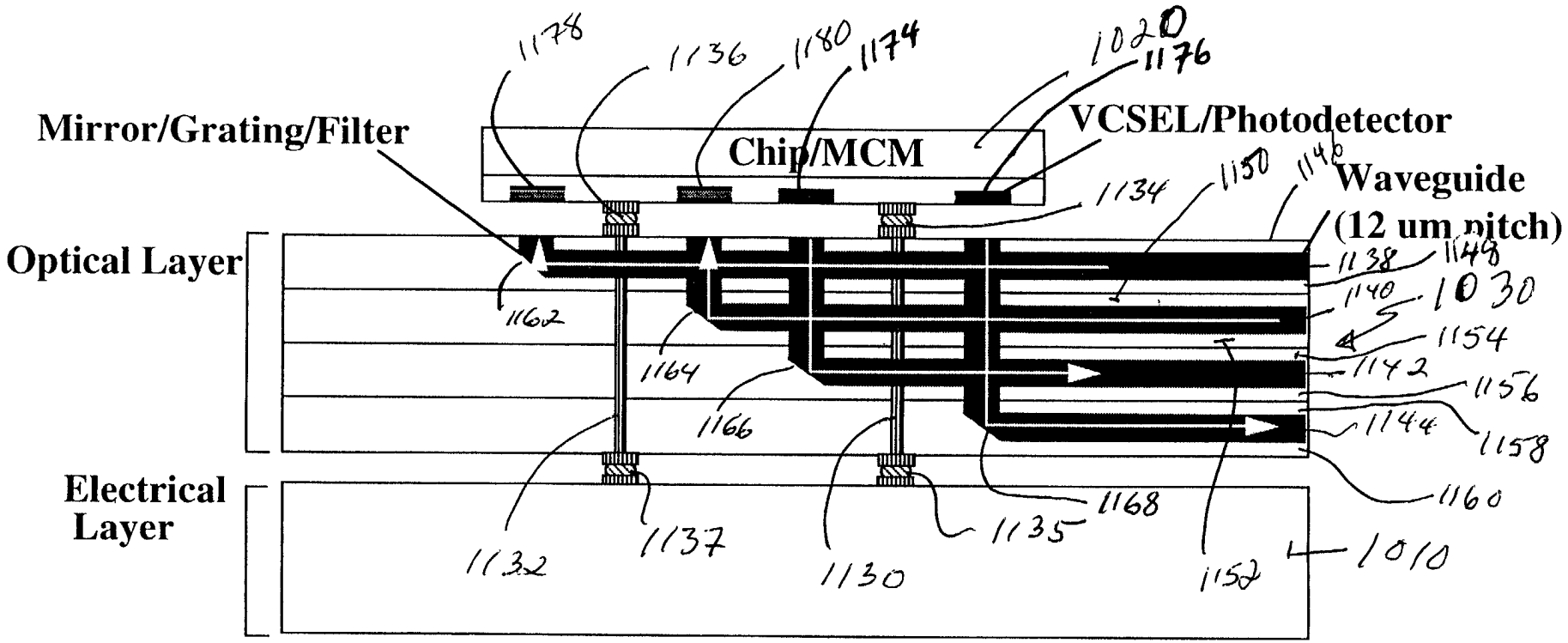


Fig 185

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

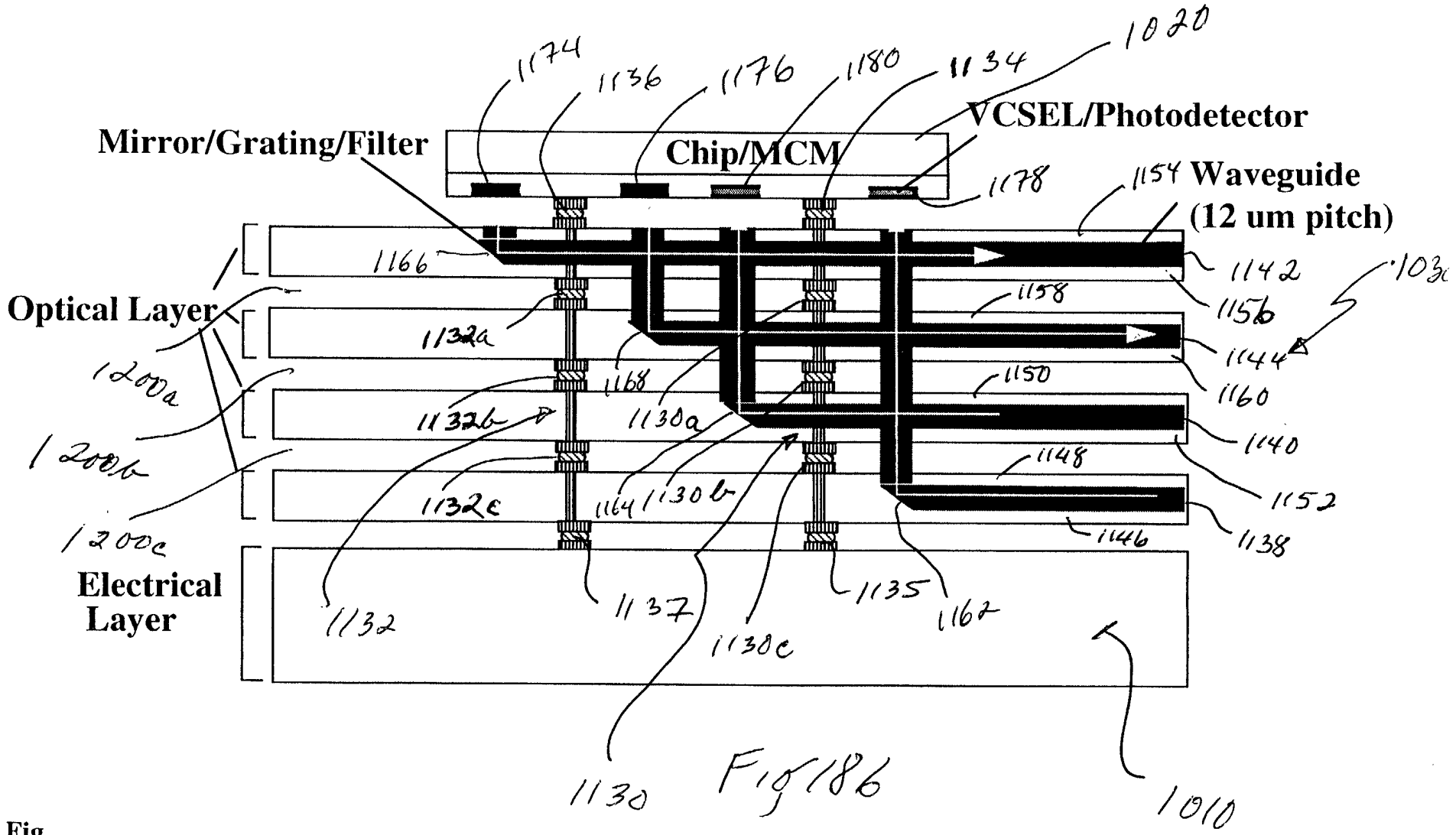


Fig. Fig 186

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

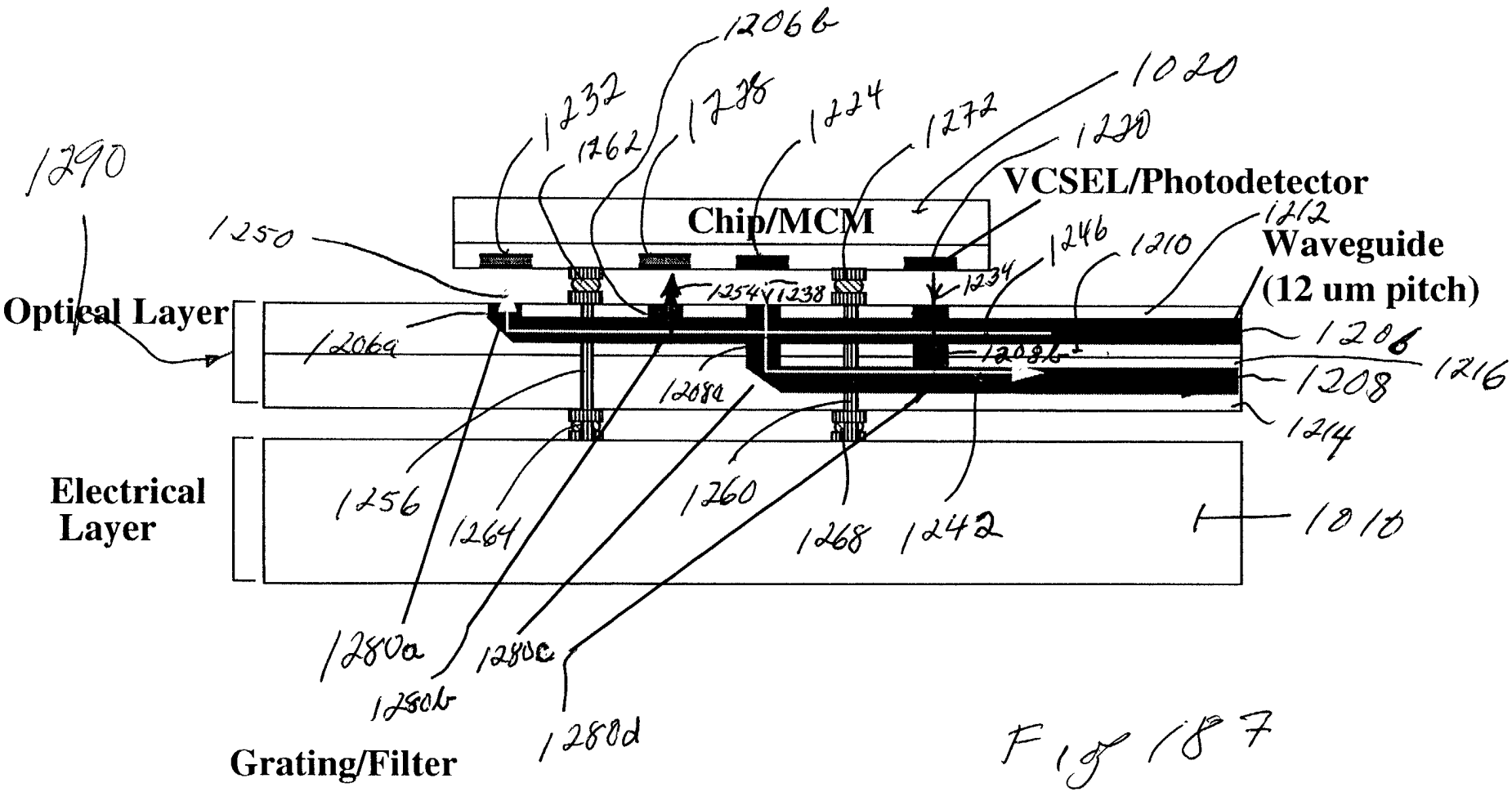


Fig 187

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

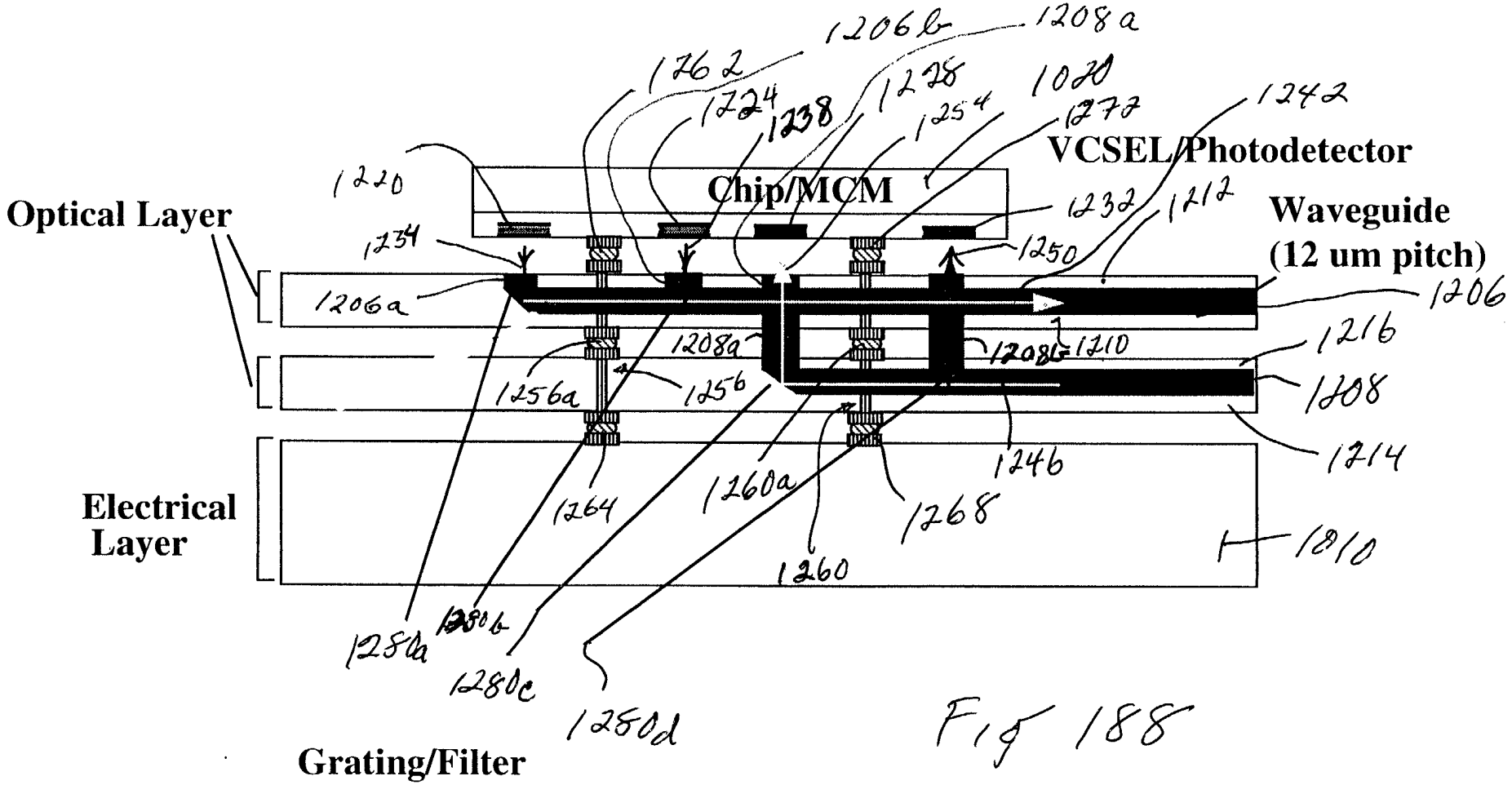


Fig 188

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

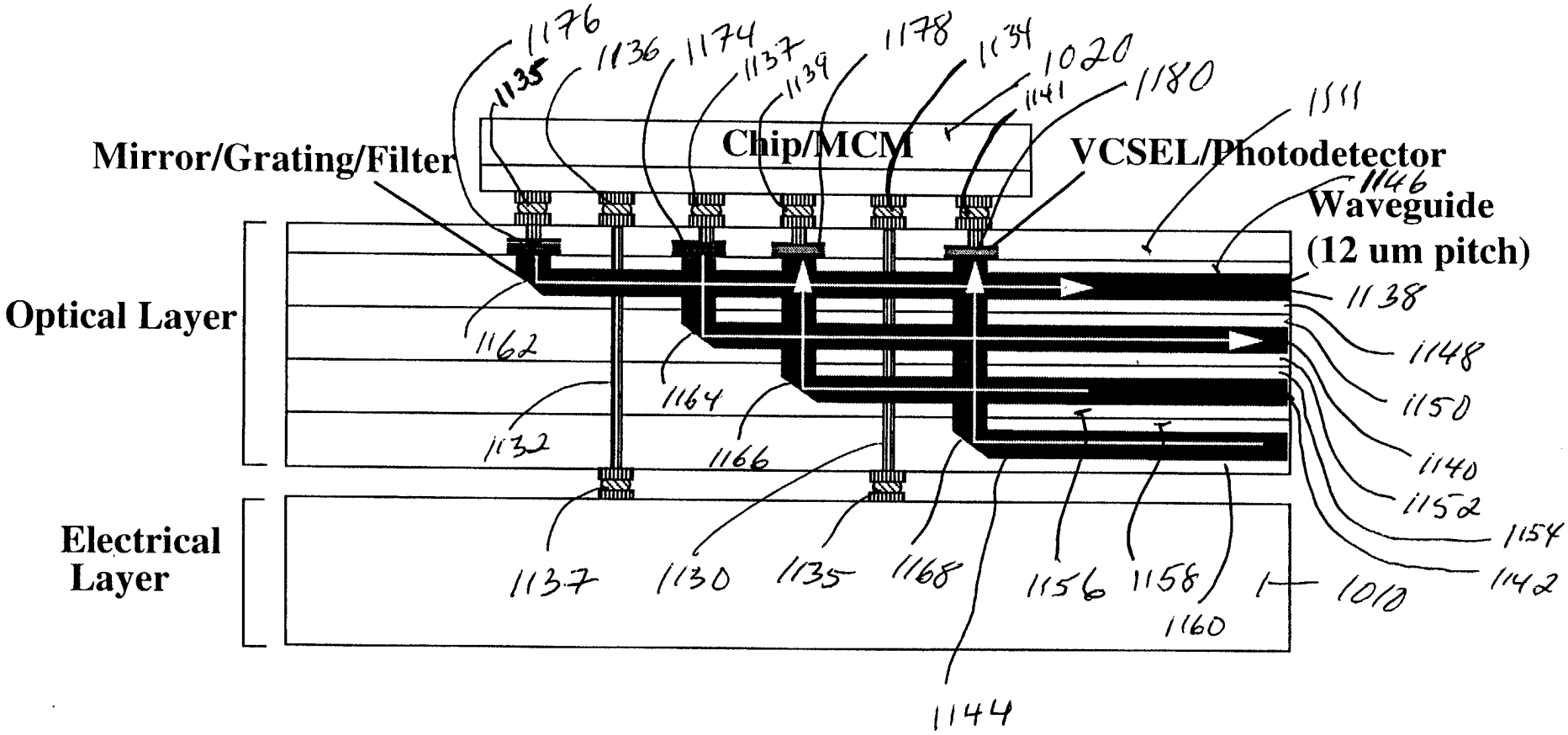


Fig 189

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

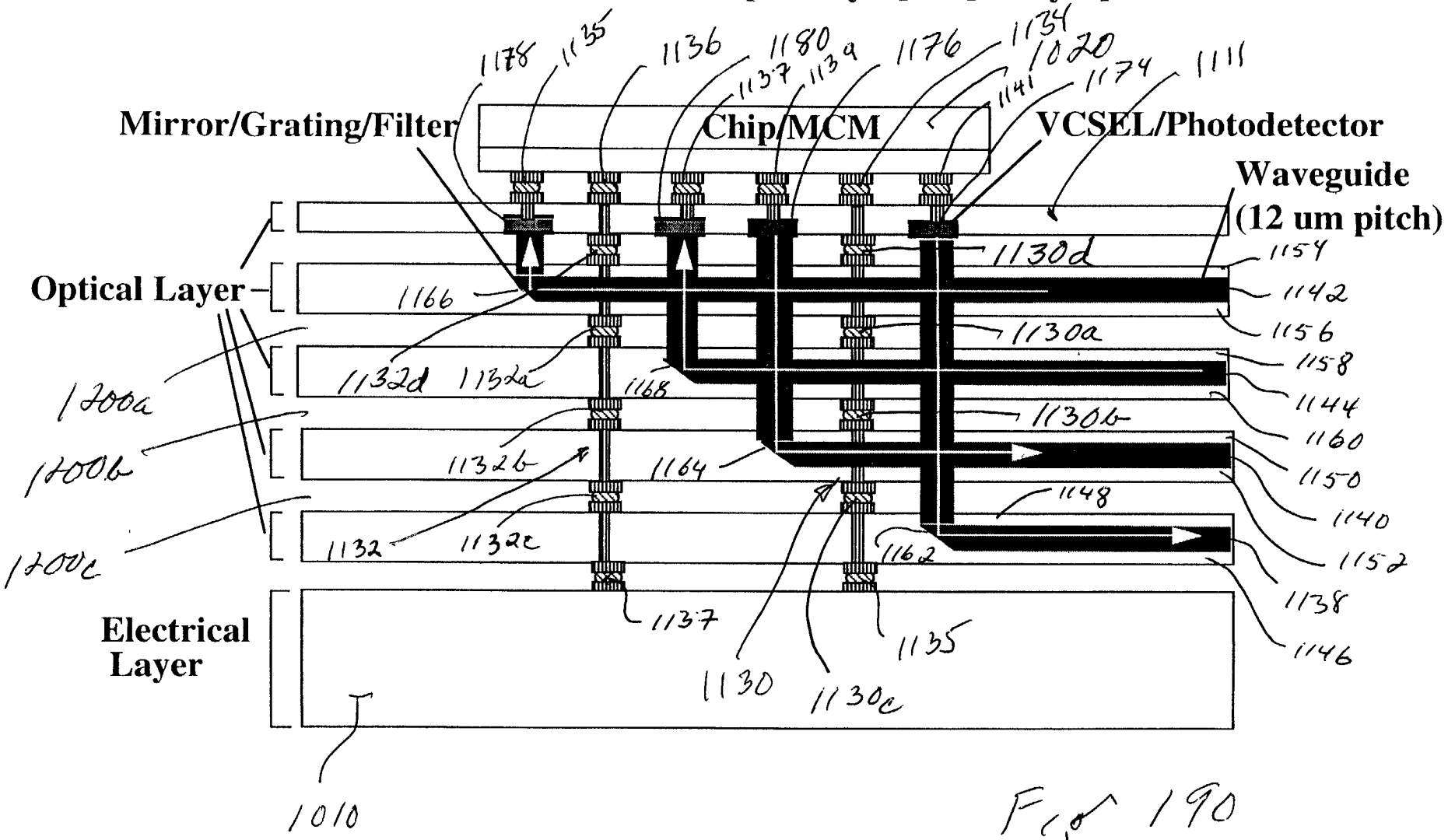


Fig. 9

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer , WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

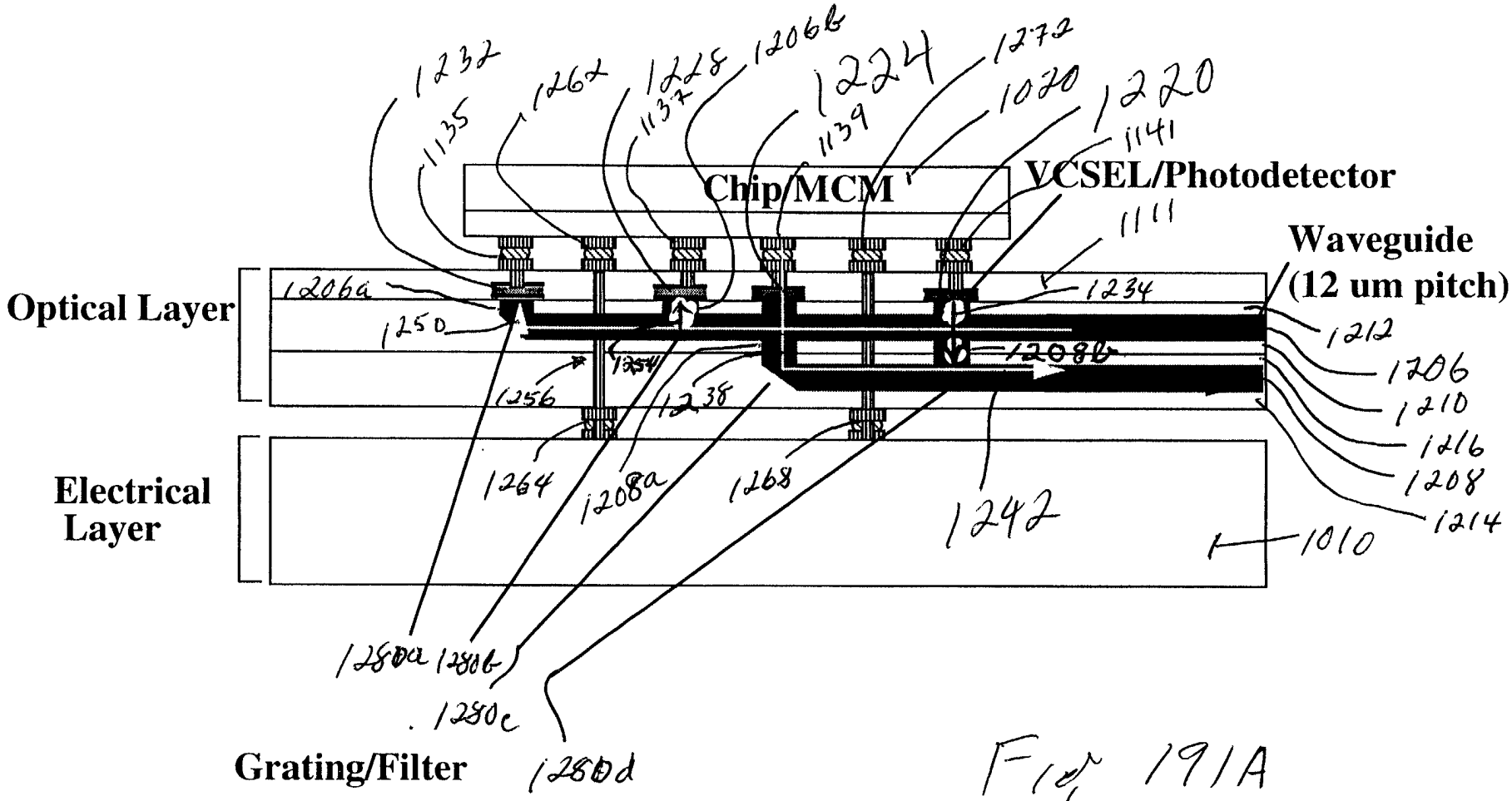


Fig 19A

Fig. 10

I/O Connection in OE Substrate (Active OE Layer , WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

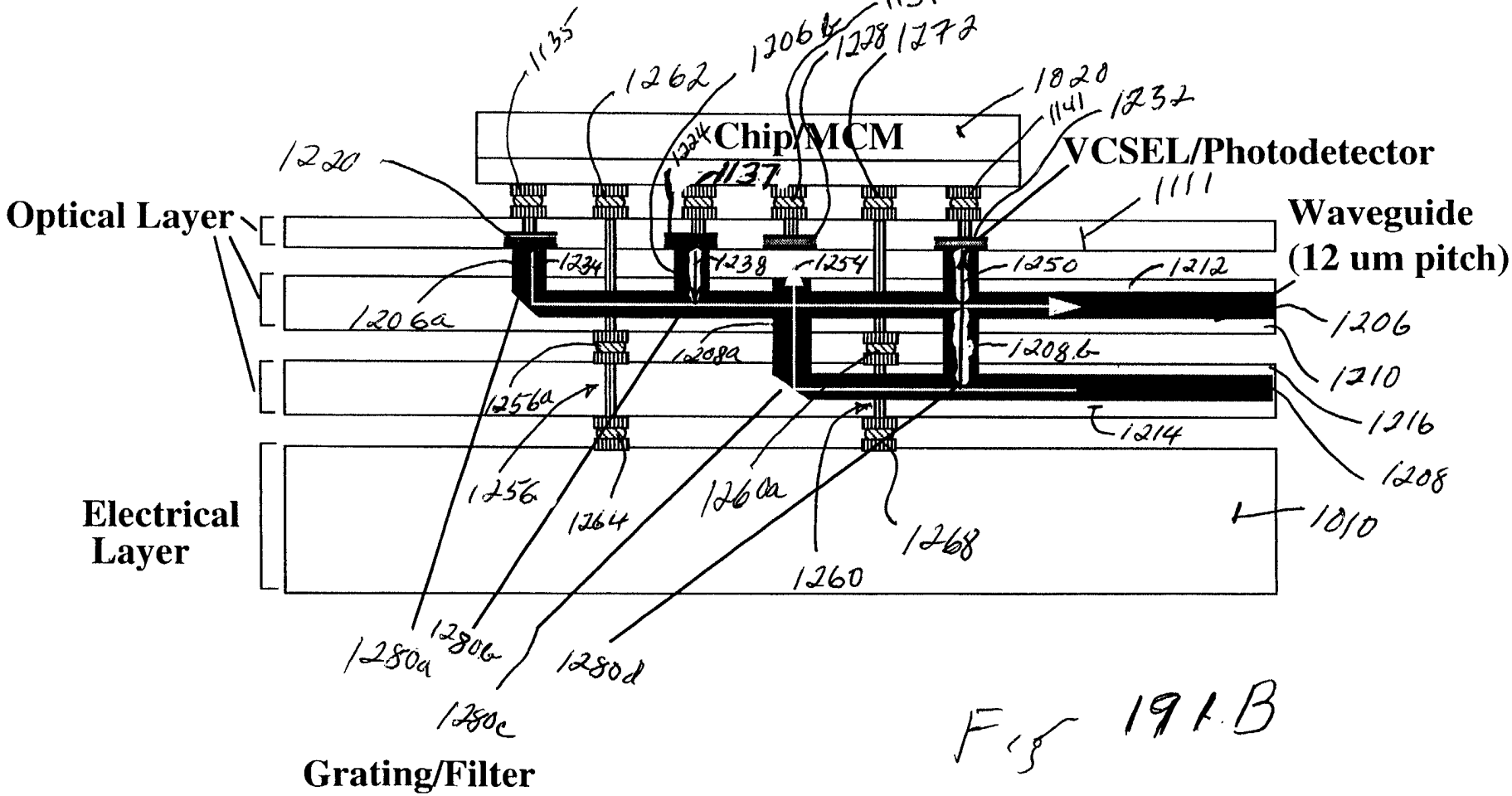


Fig 19 1.B

Fig. 11

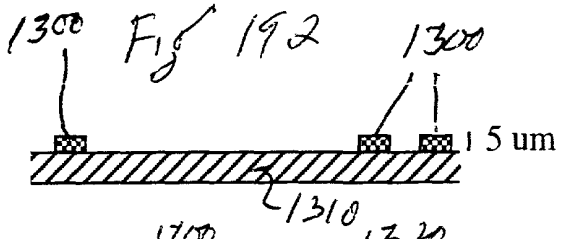


Fig 192

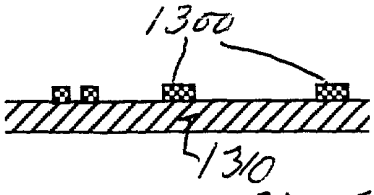


Fig 193

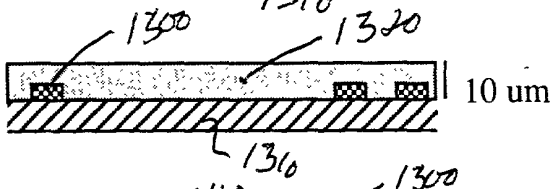


Fig 194

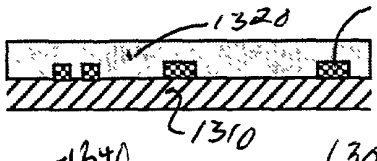


Fig 195

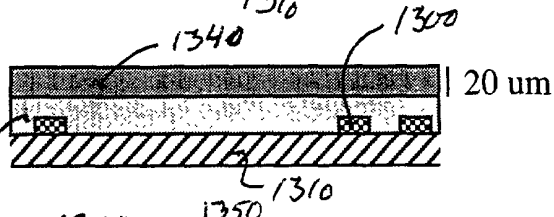


Fig 196

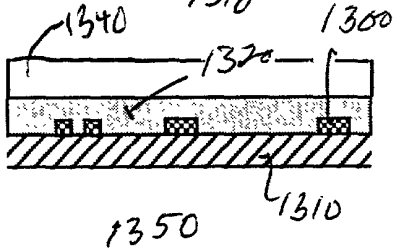


Fig 197

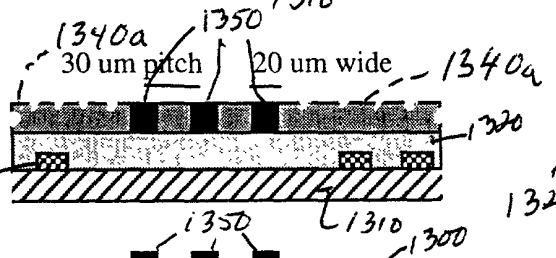


Fig 198

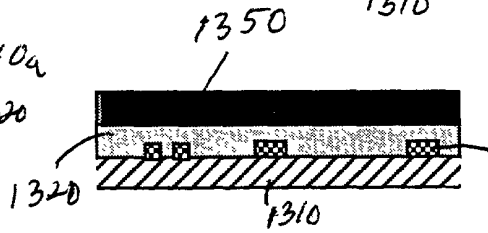


Fig 199

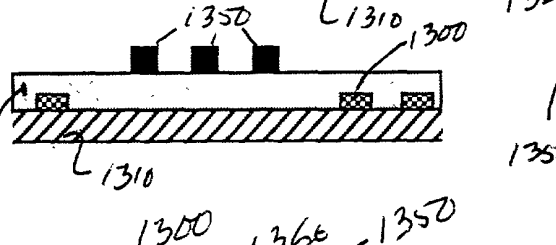


Fig 200

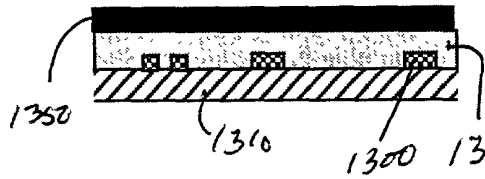


Fig 201

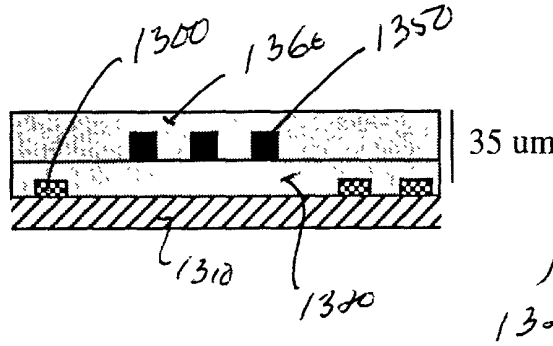


Fig 202

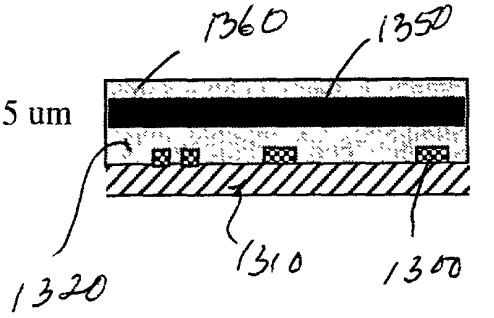


Fig 203

Fig 204

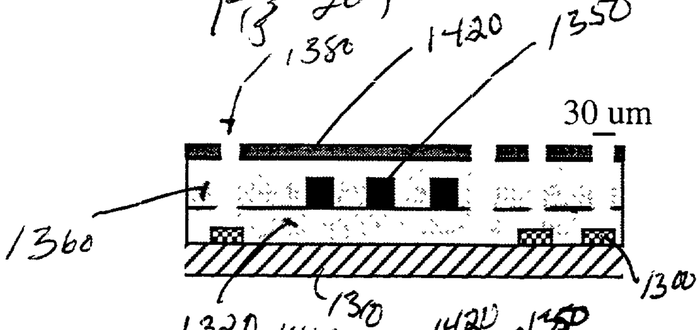


Fig 205

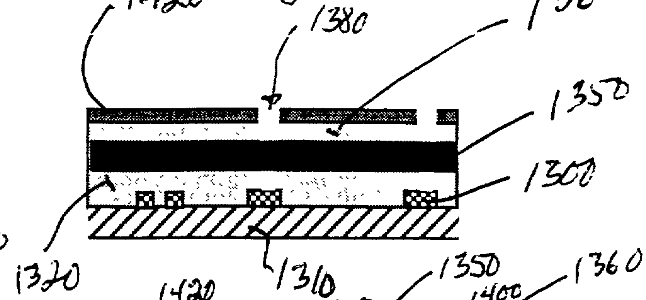


Fig 206

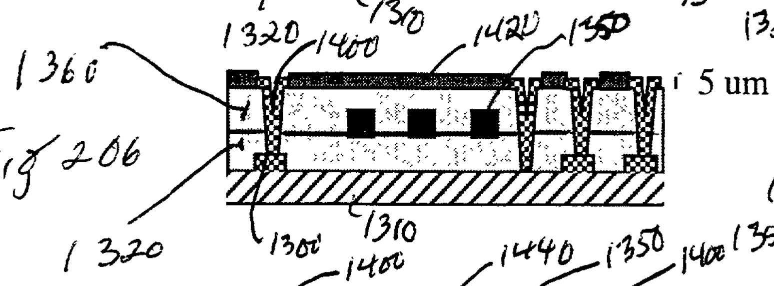


Fig 207

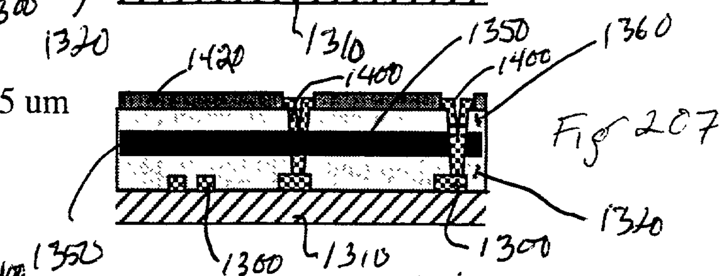


Fig 208

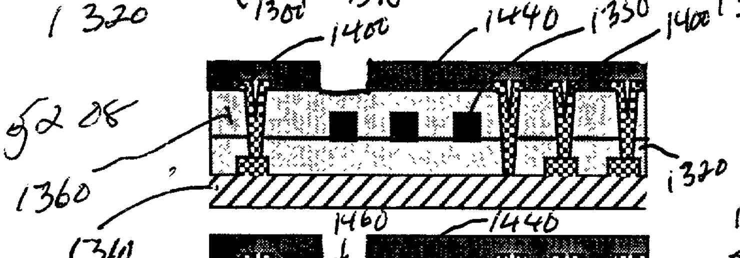


Fig 209

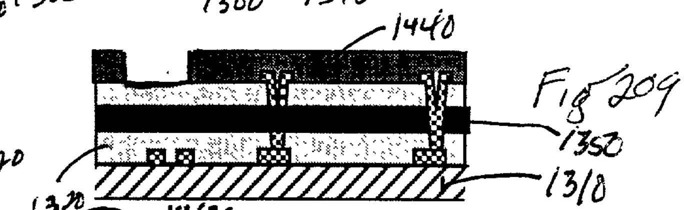


Fig 210

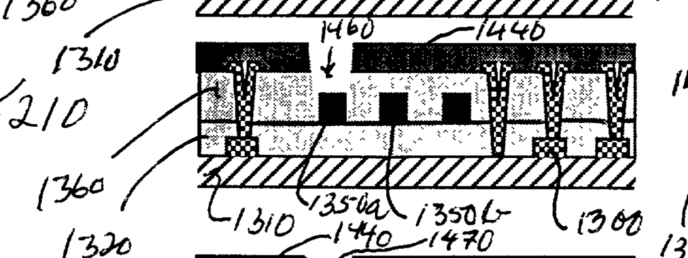


Fig 211

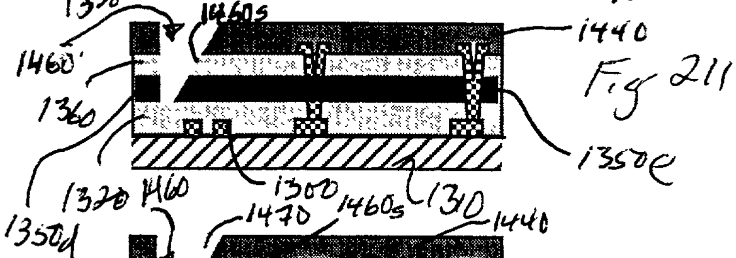


Fig 212

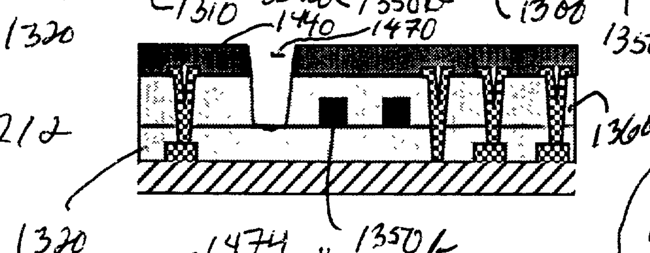


Fig 213

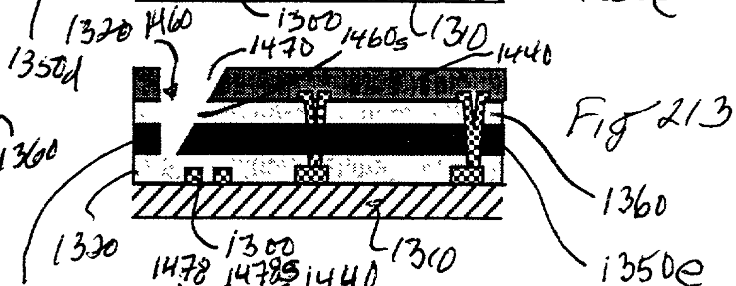


Fig 214

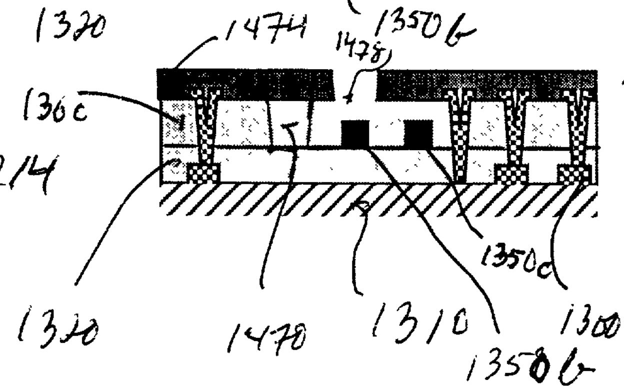
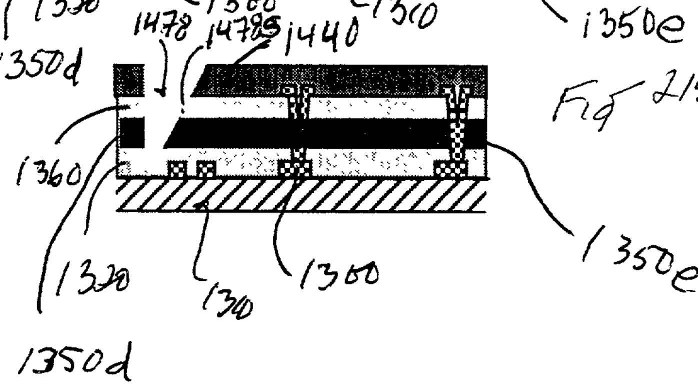


Fig 215



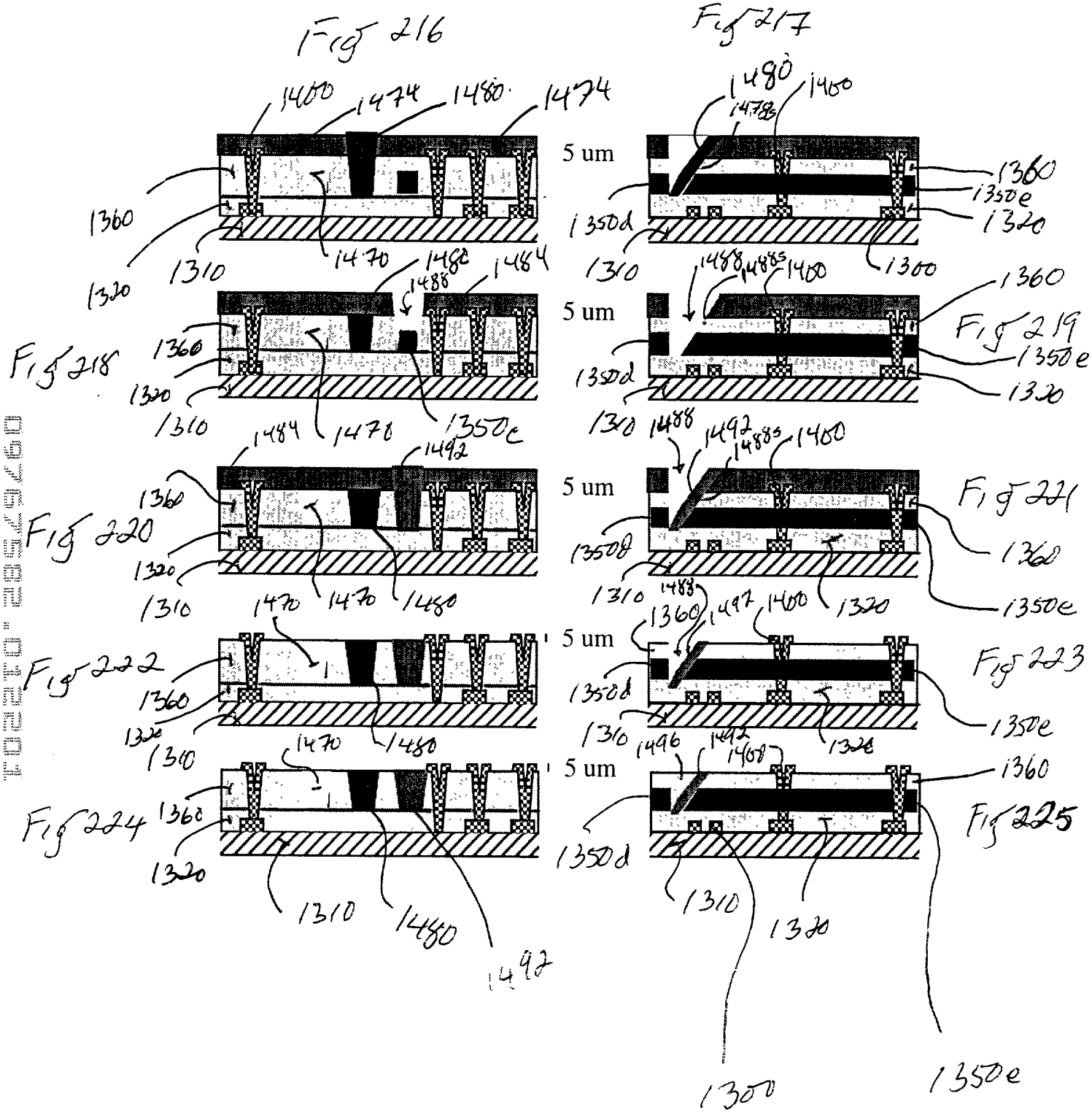


Fig 216
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Fig 226

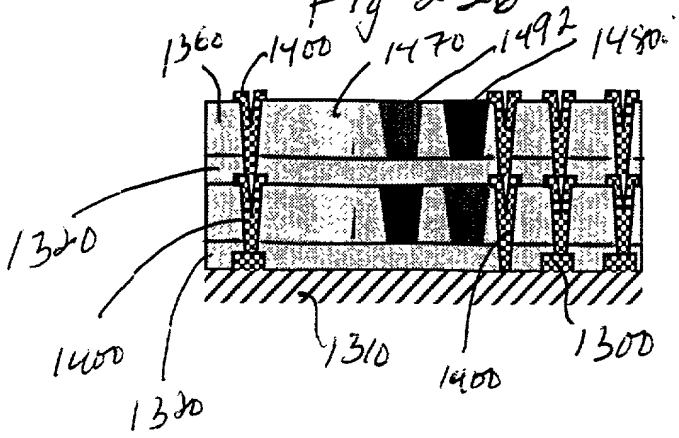


Fig 227

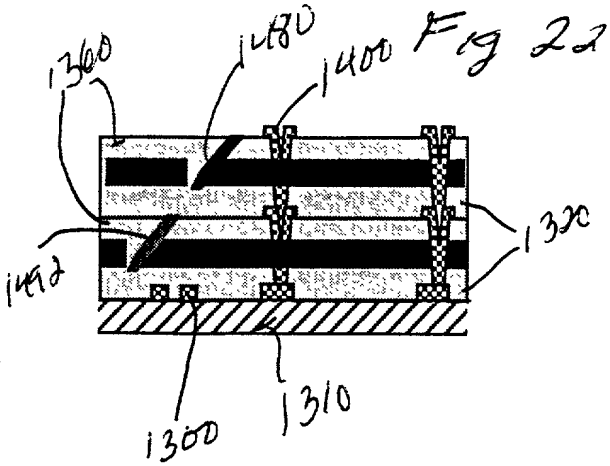


Fig 228

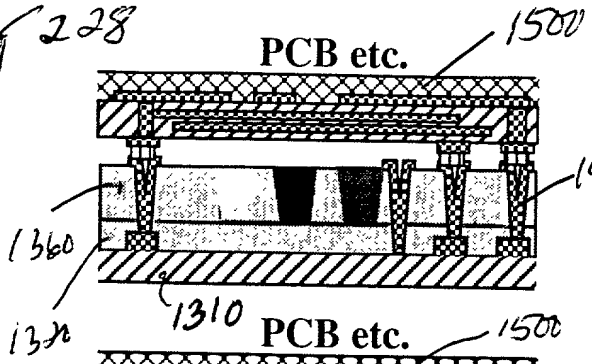
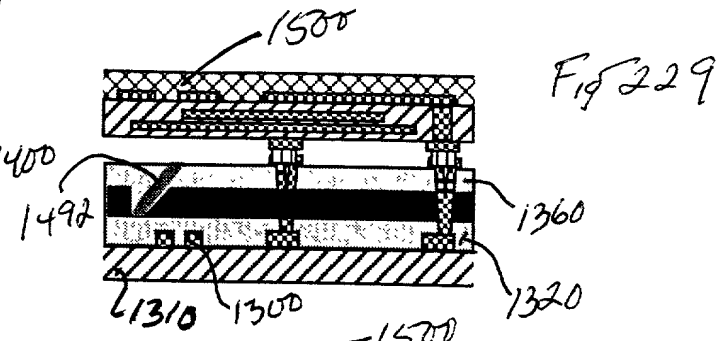


Fig 229



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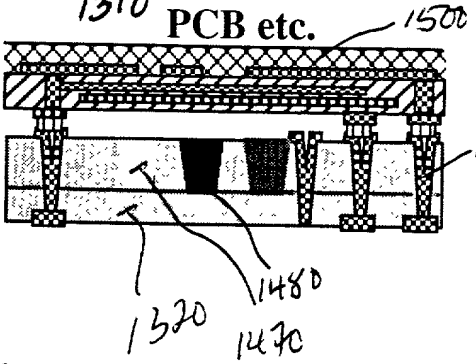


Fig 231

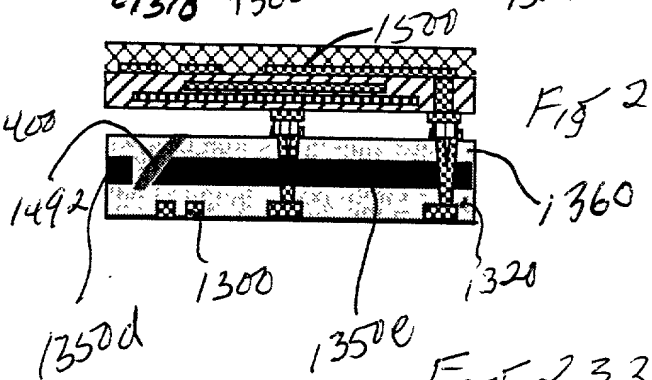
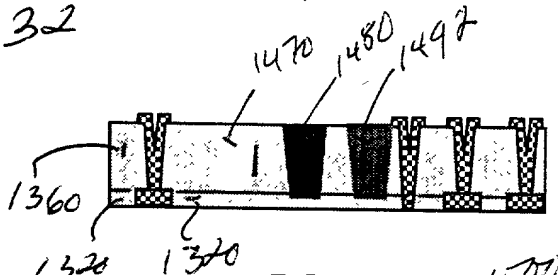


Fig 232



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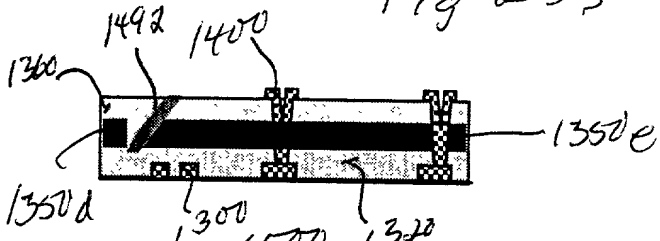

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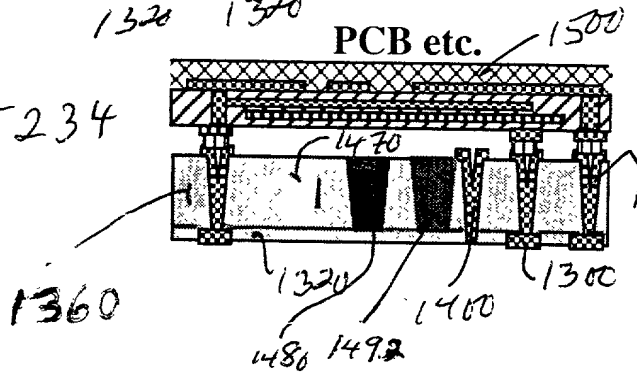
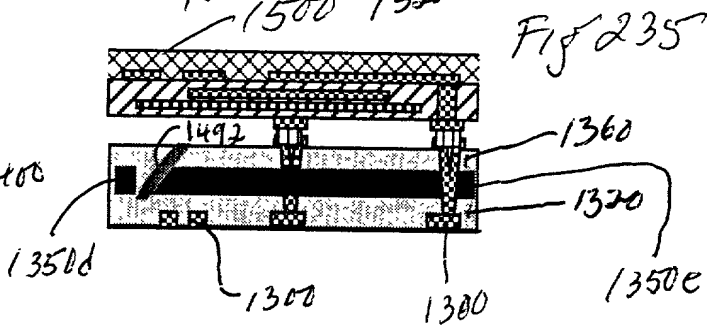


Fig 235



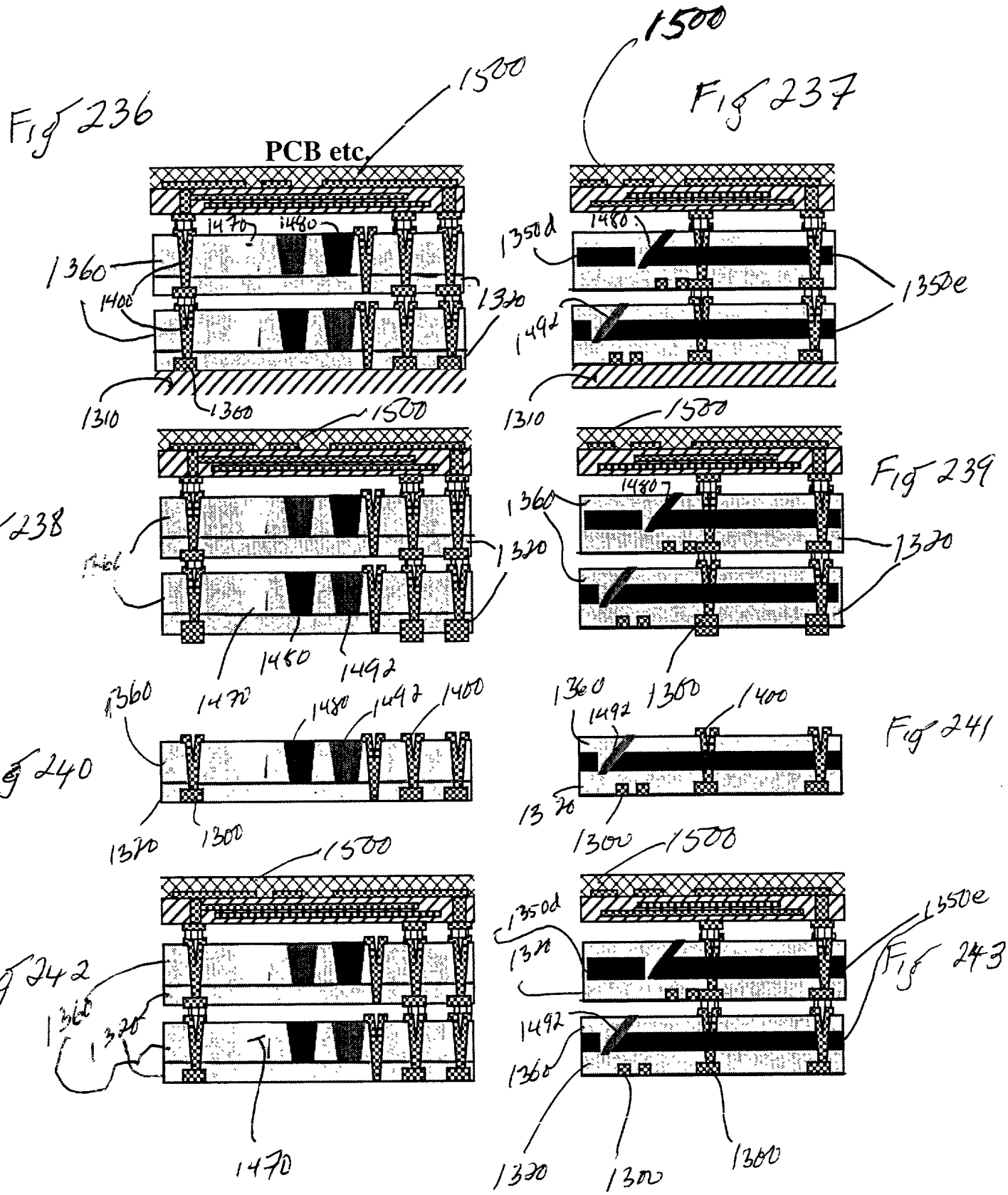


Fig 236
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Fig 244

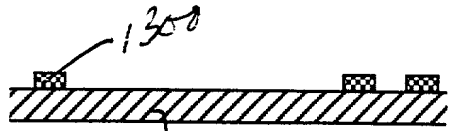


Fig 245

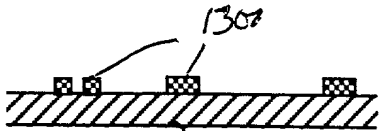


Fig 246

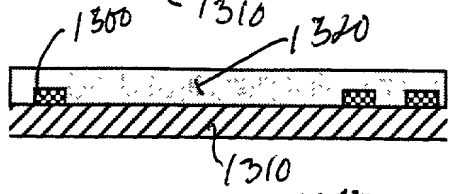


Fig 247

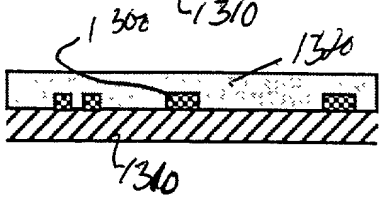


Fig 248

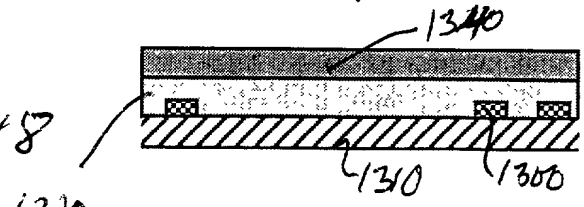


Fig 249

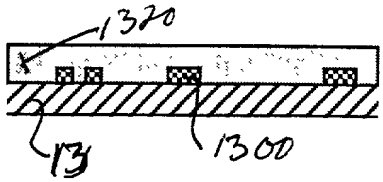


Fig 250

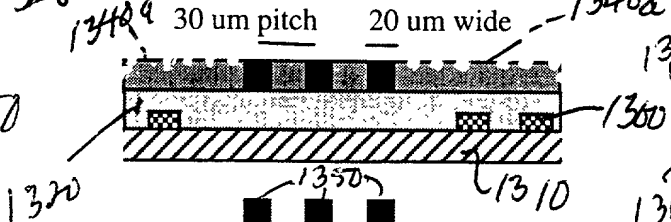


Fig 251

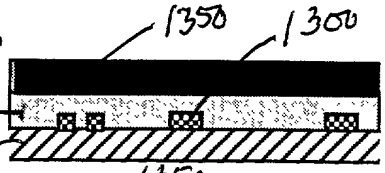


Fig 252

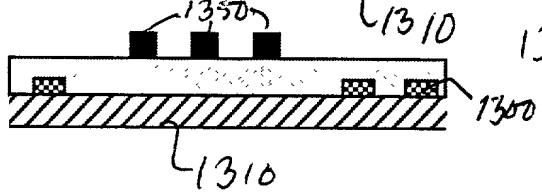


Fig 253

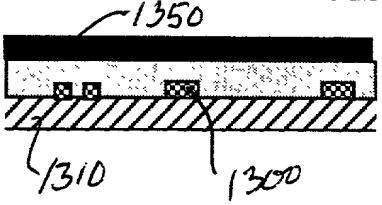


Fig 254

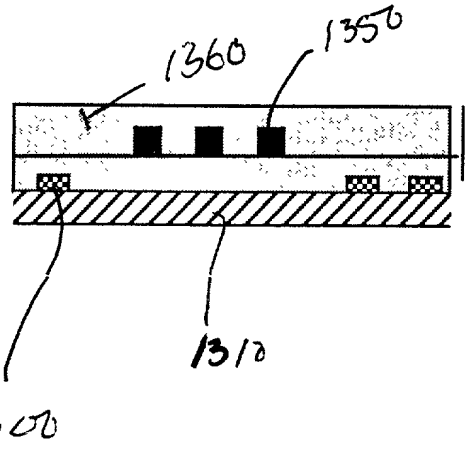
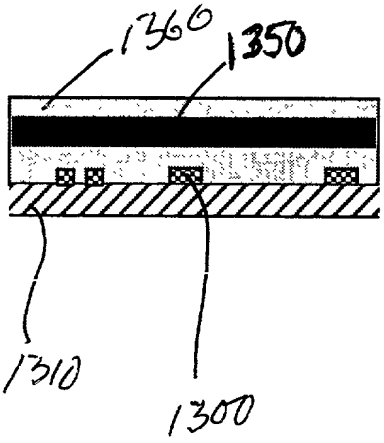


Fig 255



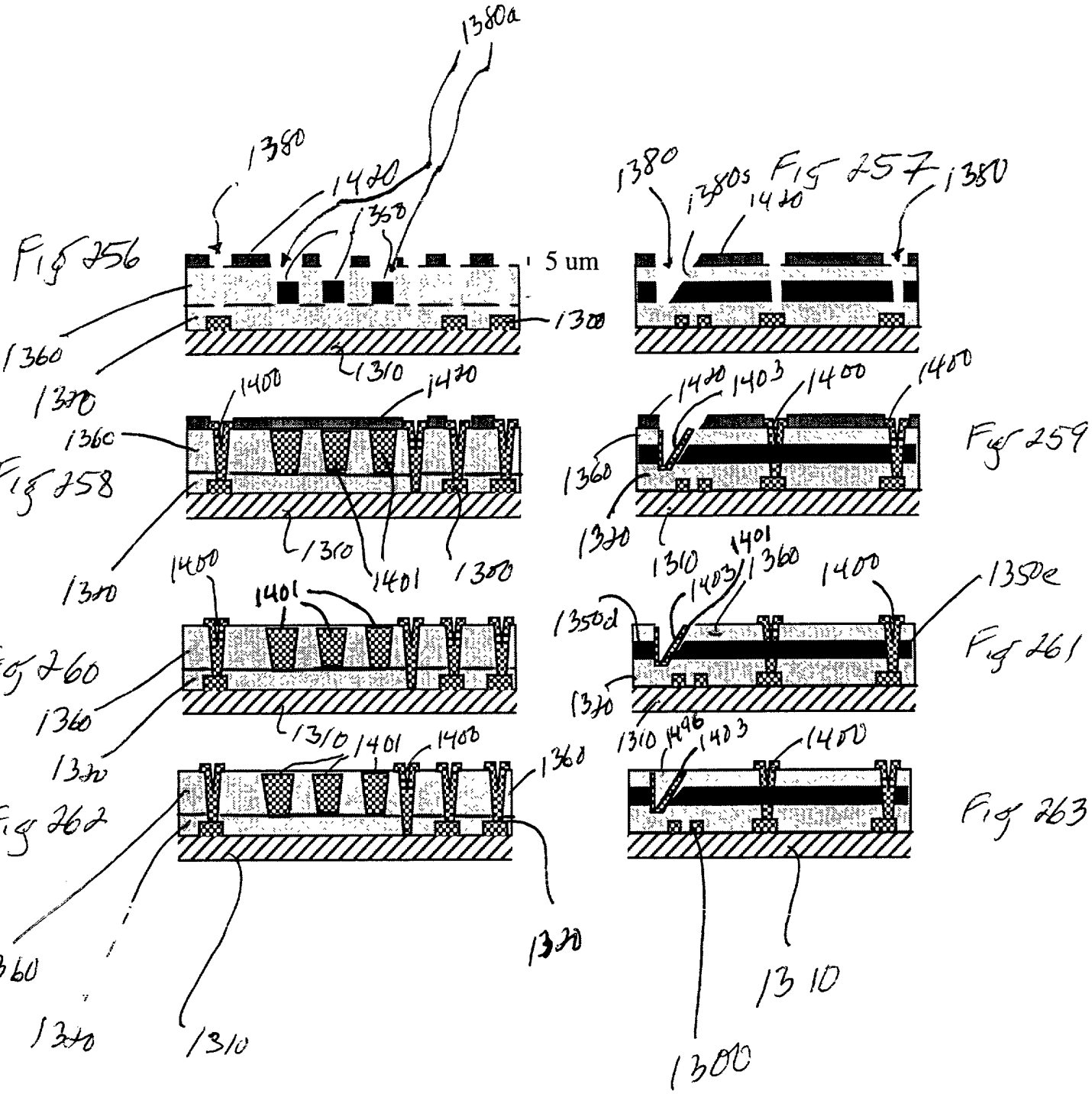

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Fig 258
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Fig 260
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Fig 263

Fig 264

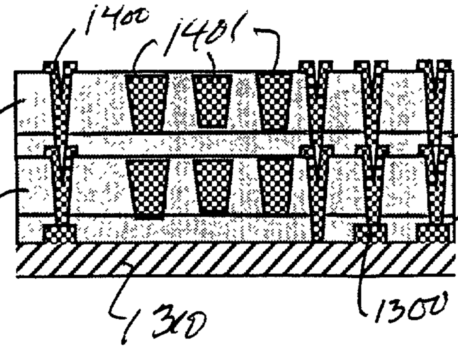


Fig 265

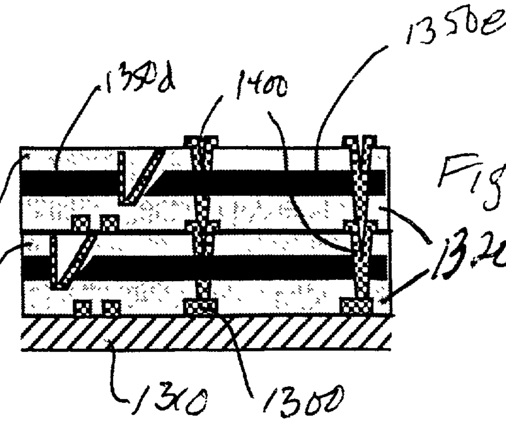


Fig 266

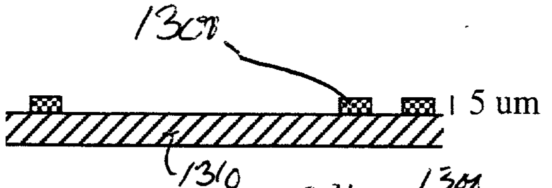


Fig 267

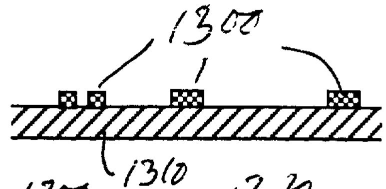


Fig 268

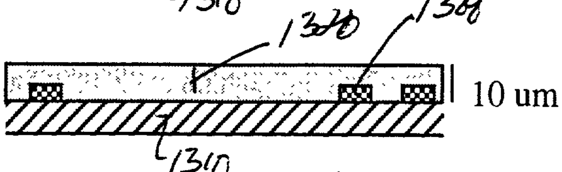


Fig 269

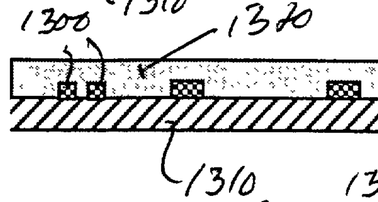


Fig 270

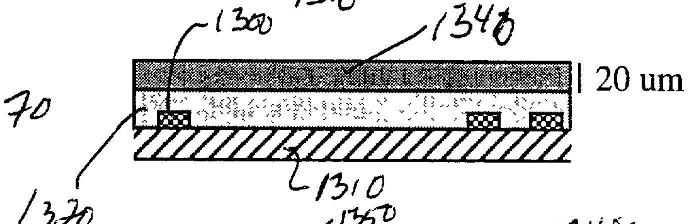


Fig 271

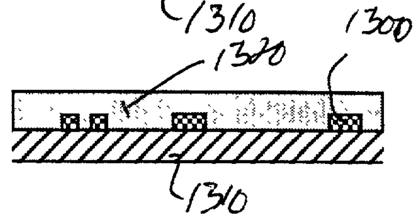


Fig 272

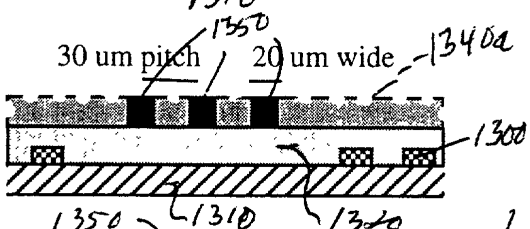


Fig 273

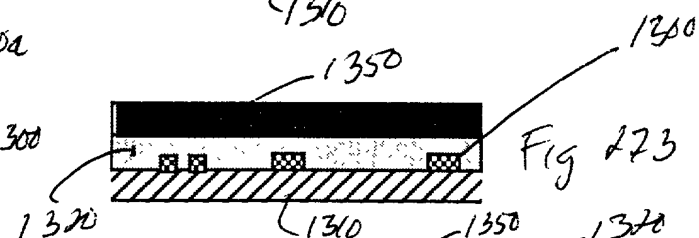


Fig 274

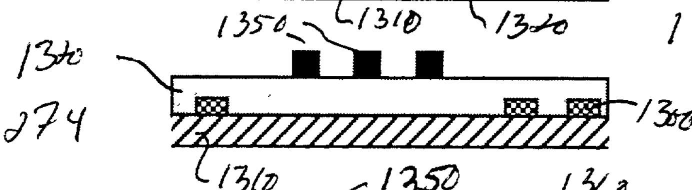


Fig 275

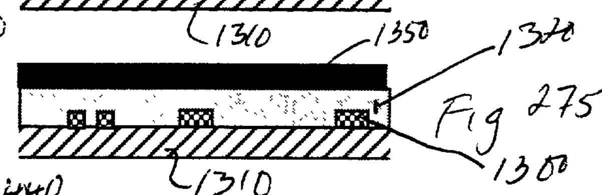


Fig. 276

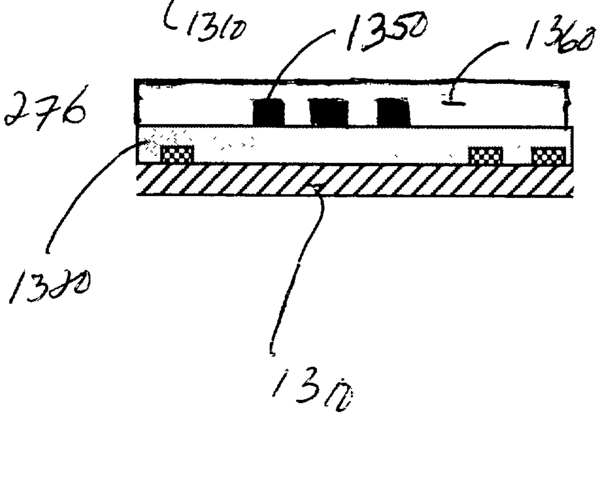
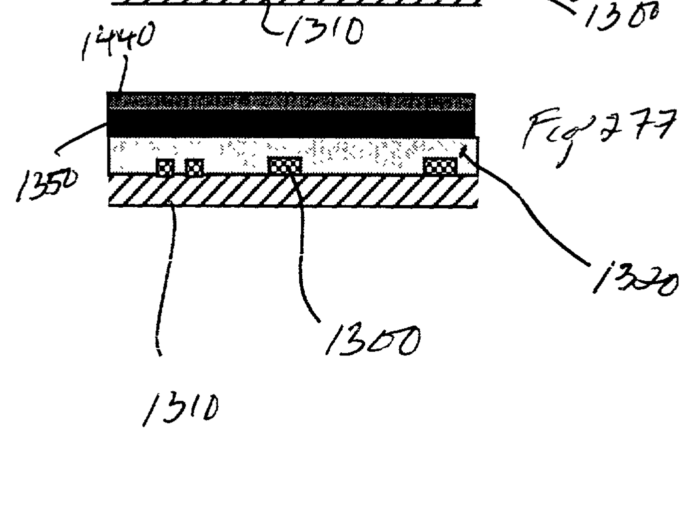


Fig 277



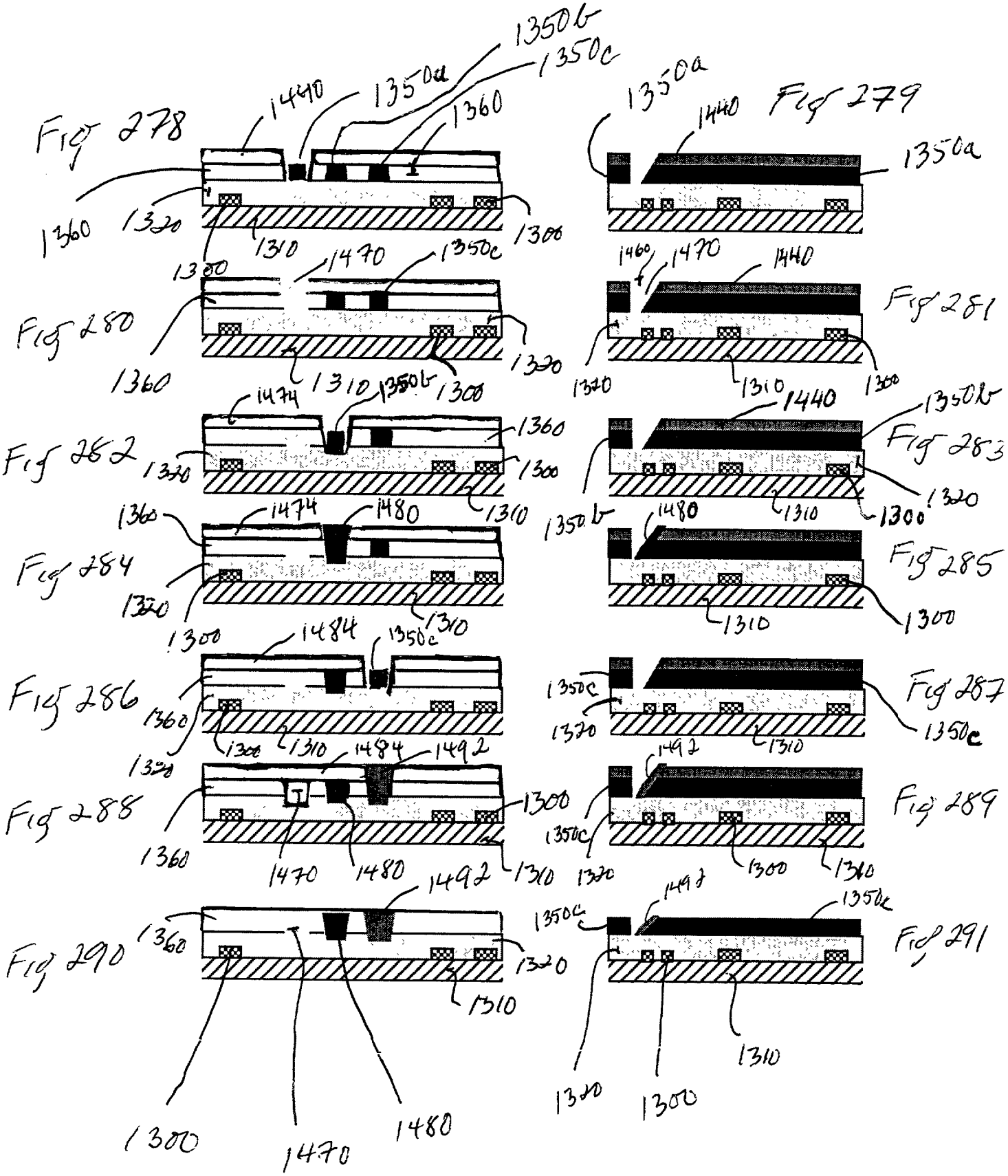


Fig 278
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Fig 279
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Fig 280
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Fig 281
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Fig 282
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1350b
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Fig 283
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Fig 285
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Fig 286
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Fig 287
1350c
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Fig 288
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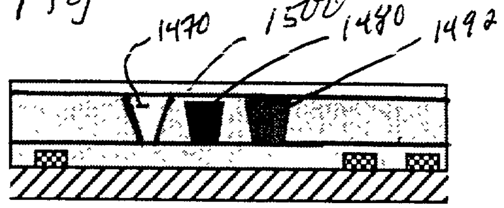

Fig 292

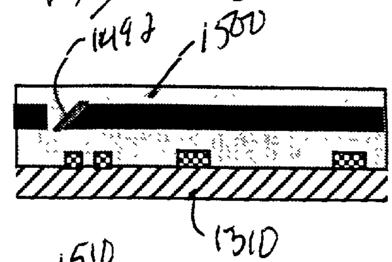

Fig 293

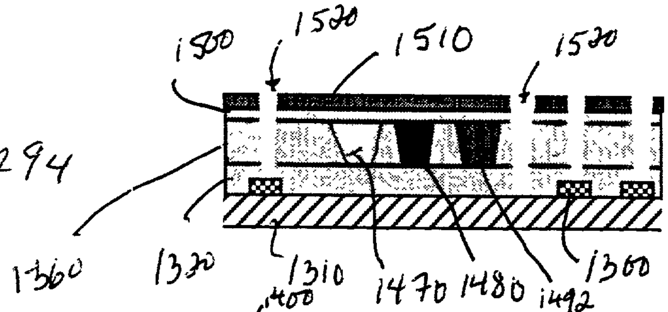

Fig 294

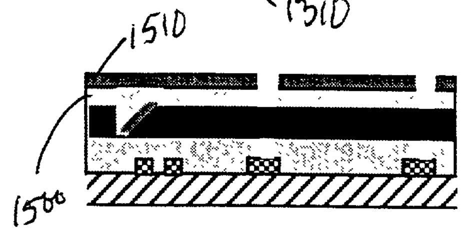

Fig 295

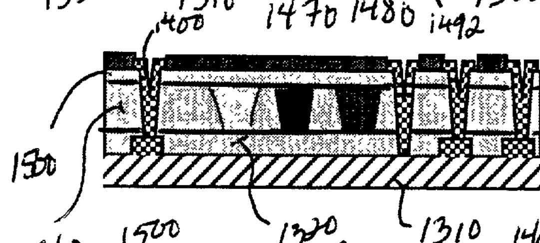

Fig 296

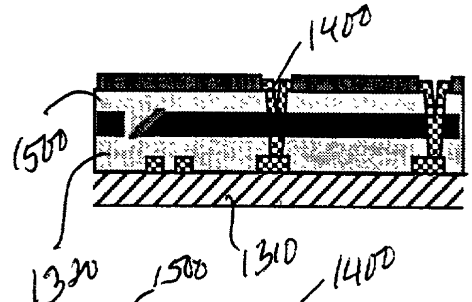

Fig 297

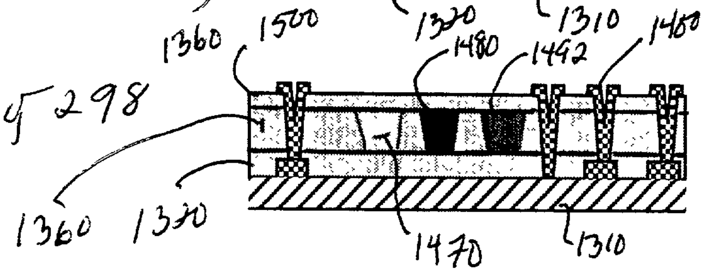

Fig 298

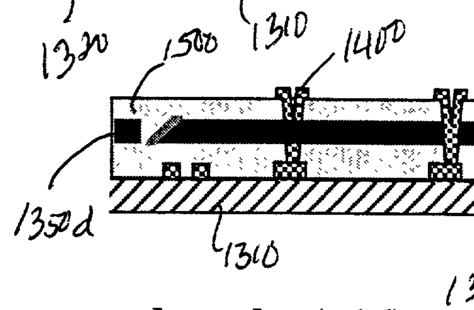

Fig 299

In the case of multi layer (a1-a16) process is repeated on the (a16).
-it is also possible to repeat (a3-a16) or (a1, a3-a16)

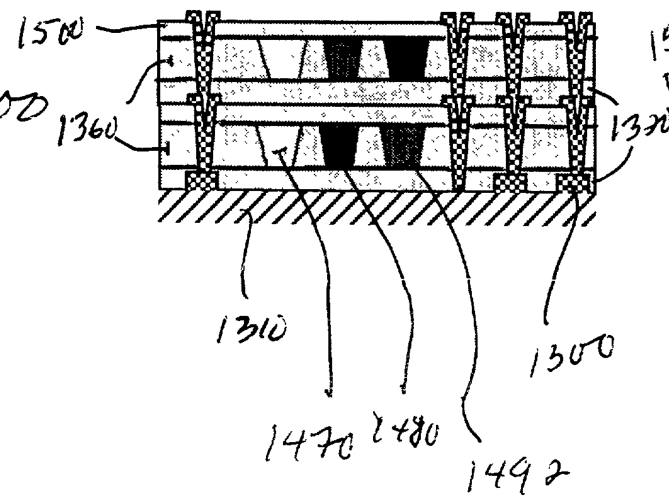

Fig 300

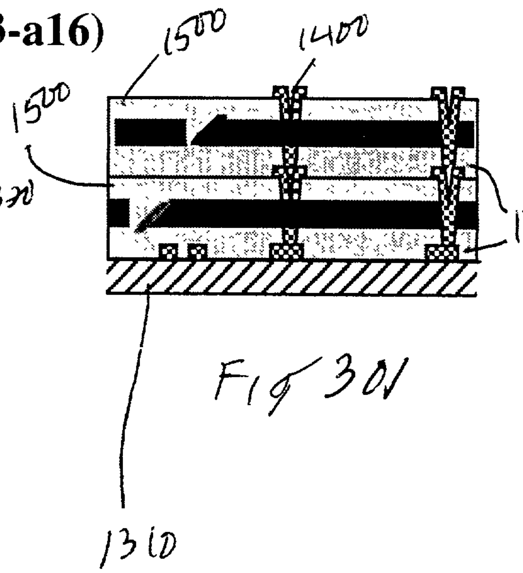

Fig 301

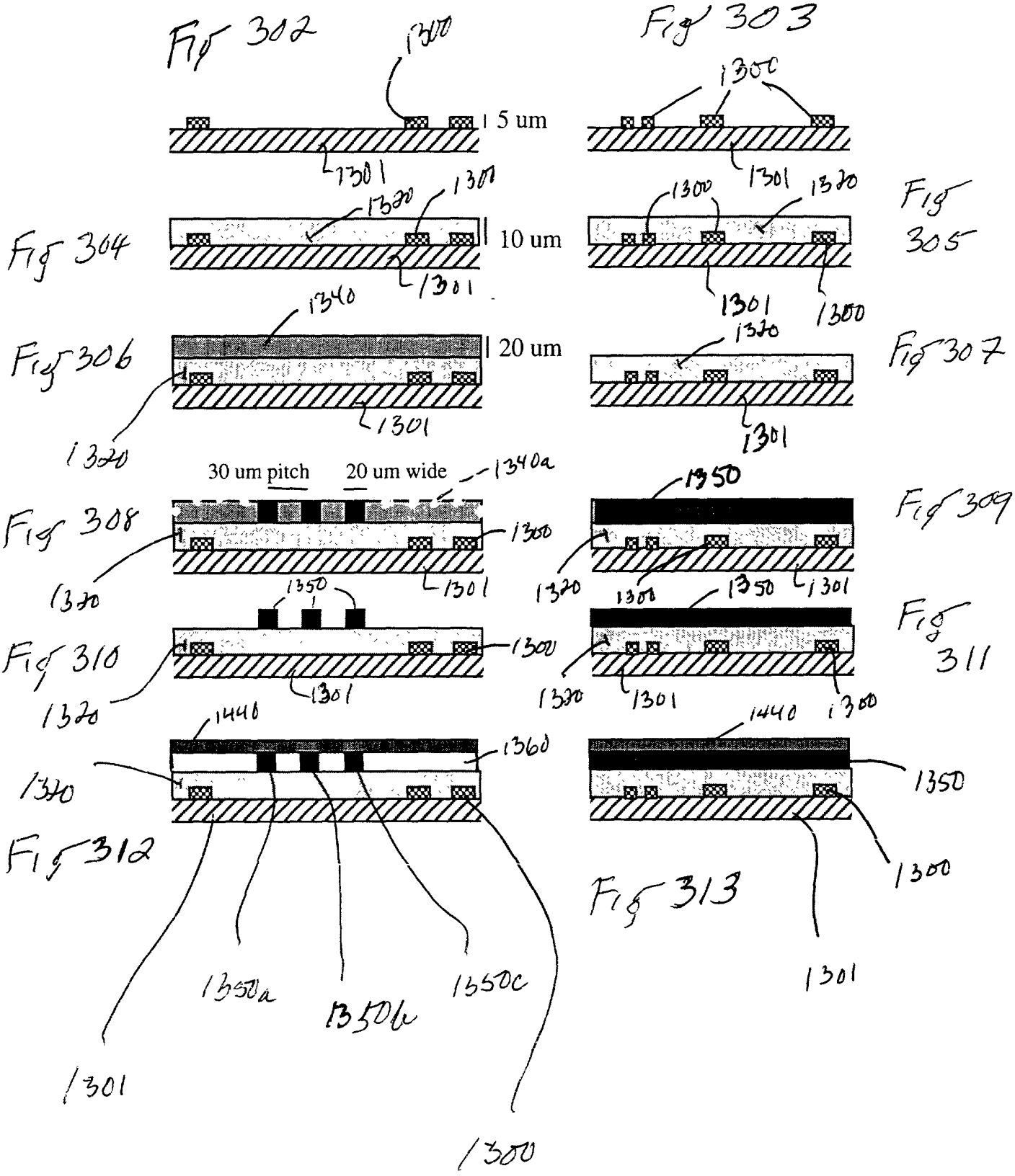
Fig 302
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Fig 307
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Fig 308
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Fig 311
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Fig 312
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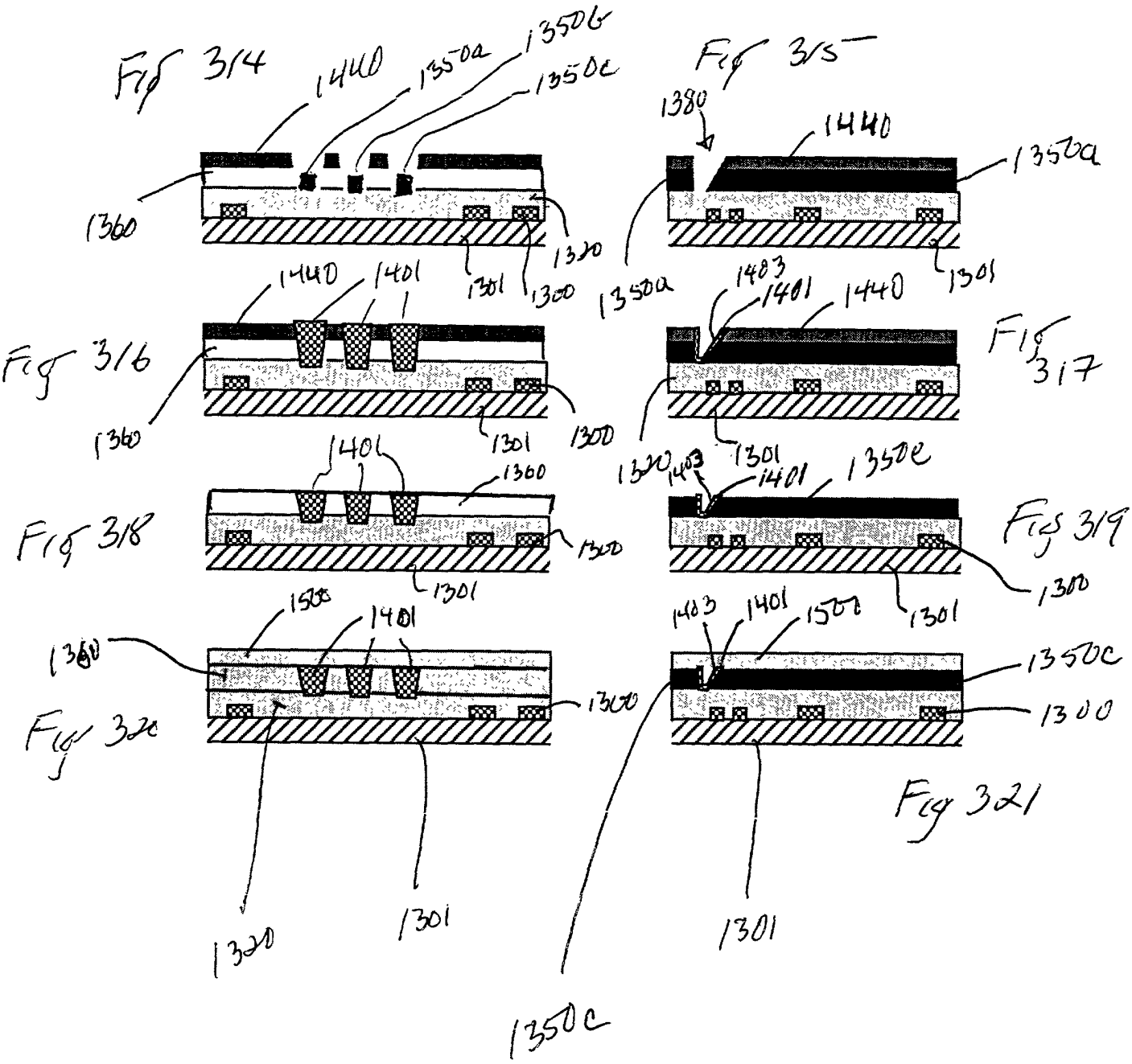
Fig 314
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Fig 315
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Fig 316
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Fig 317
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1350c
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Fig 318
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Fig 319
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Fig 321
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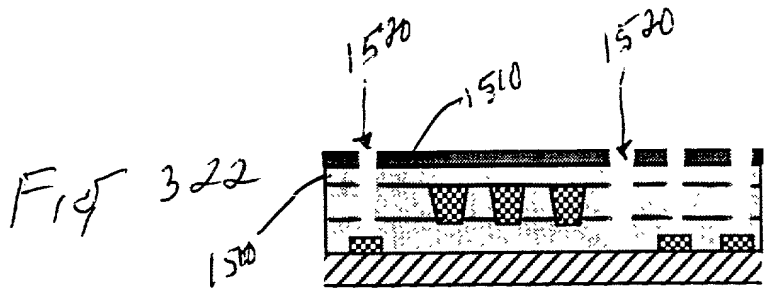


Fig 322

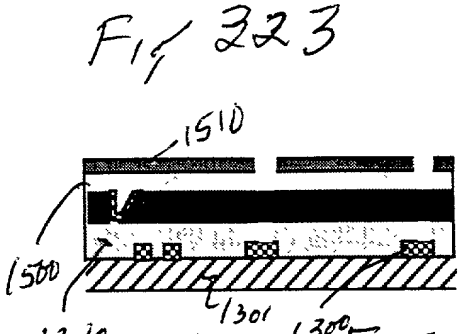


Fig 323

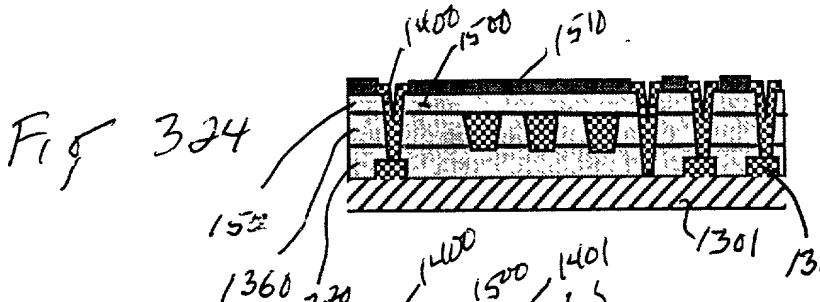


Fig 324

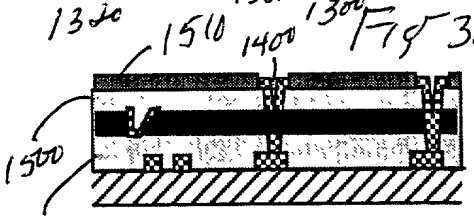


Fig 325

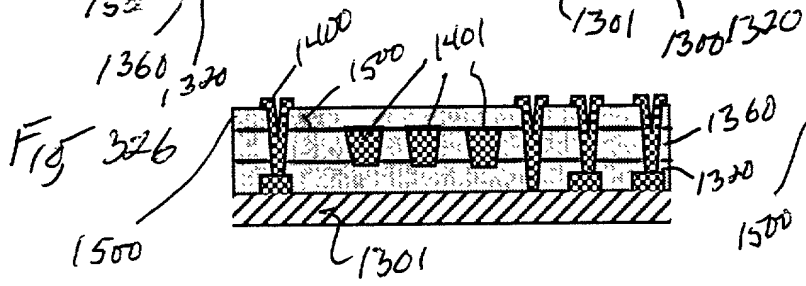


Fig 326

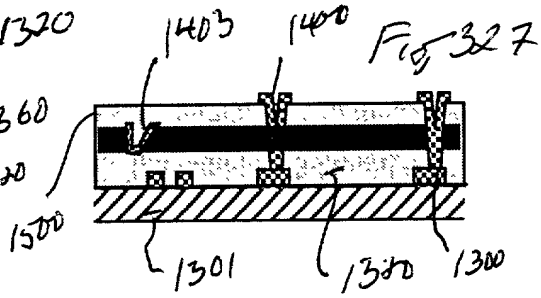


Fig 327

In the case of multi layer (a1-a12) process is repeated on the (a12).
-it is also possible to repeat (a3-a12) or (a1, a3-a12)

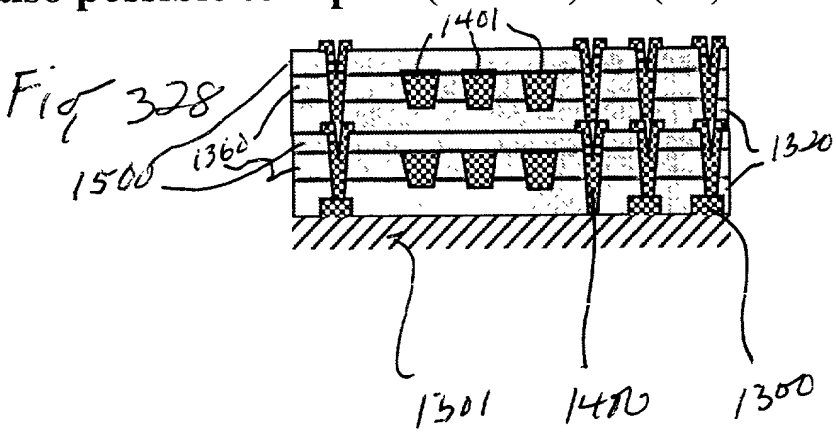


Fig 328

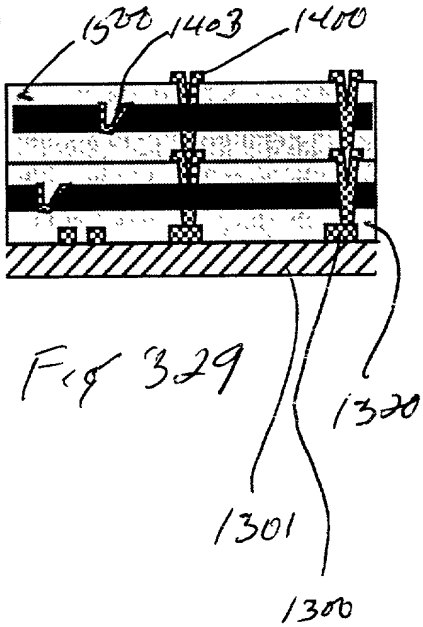


Fig 329

Invented Corner Turning Structure (A)

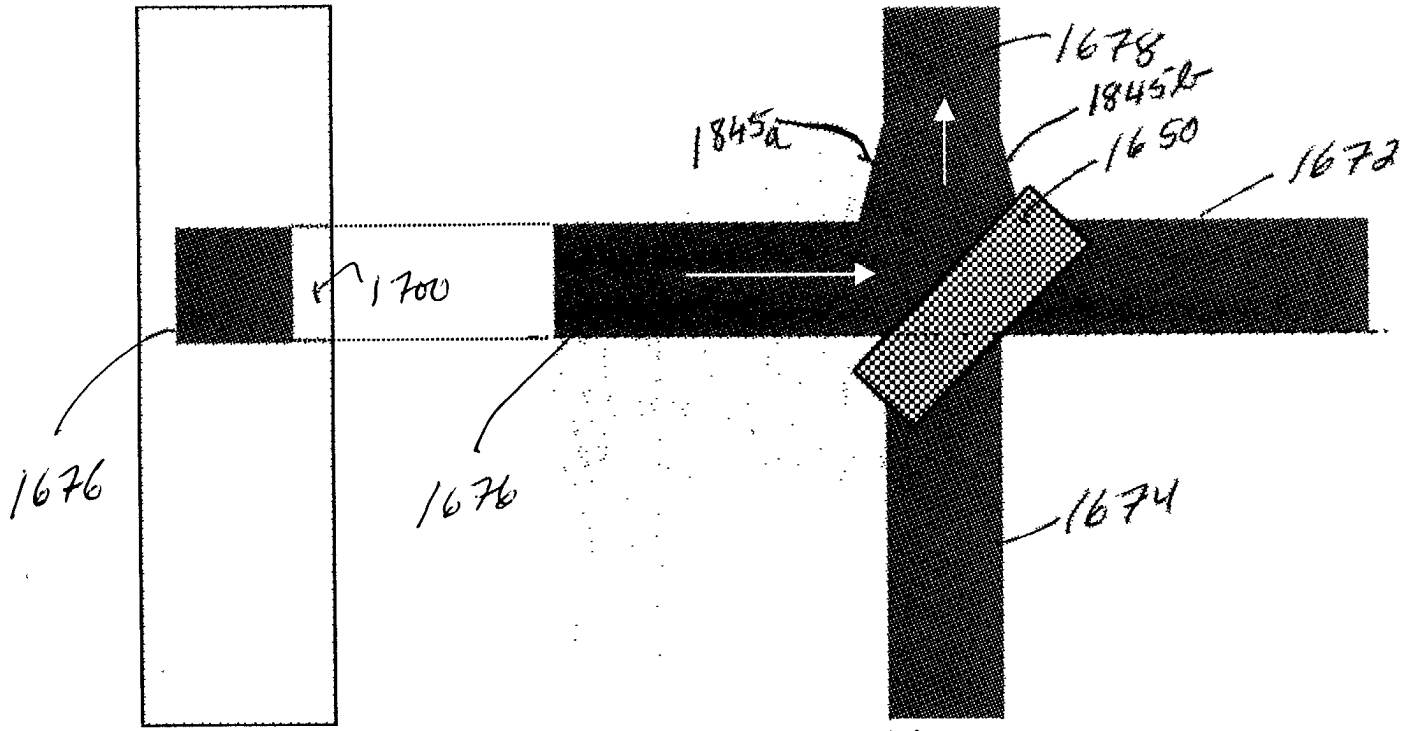


Fig 374

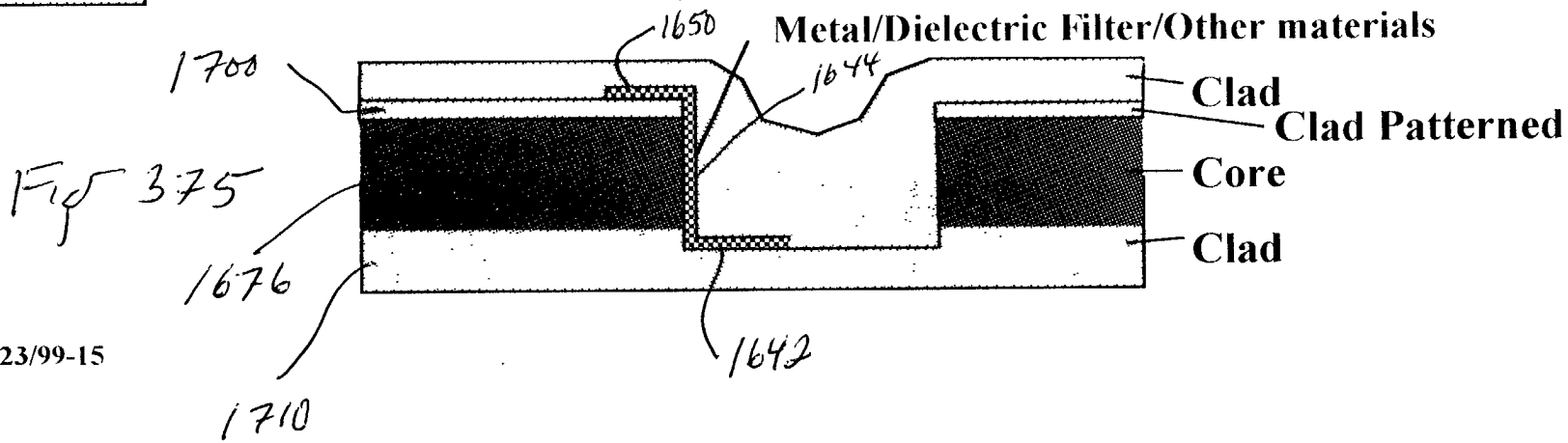
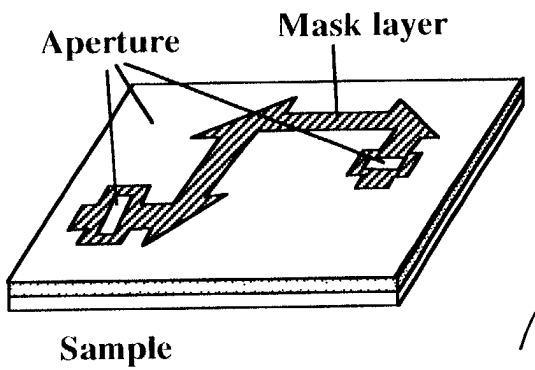


Fig 375

Fig. Add-9/23/99-15

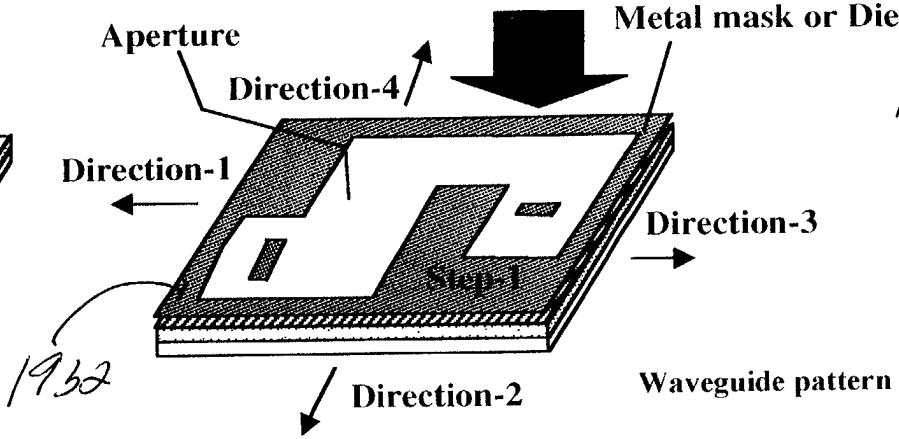
MNA, MNE Example for Add2 example

Fig 370



Excimer laser (or ion beam) with vertical incident angle

Fig 371



Waveguide pattern

Excimer laser (or ion beam) with tilted incident angle

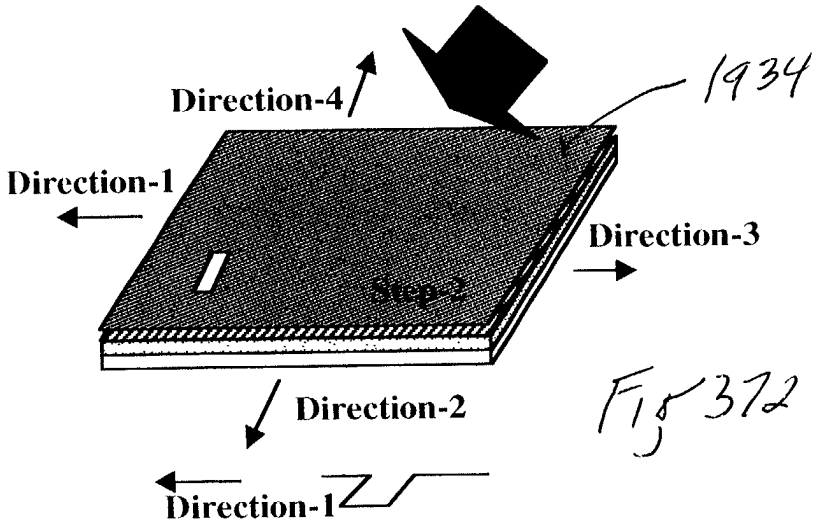


Fig 372

Fig 373

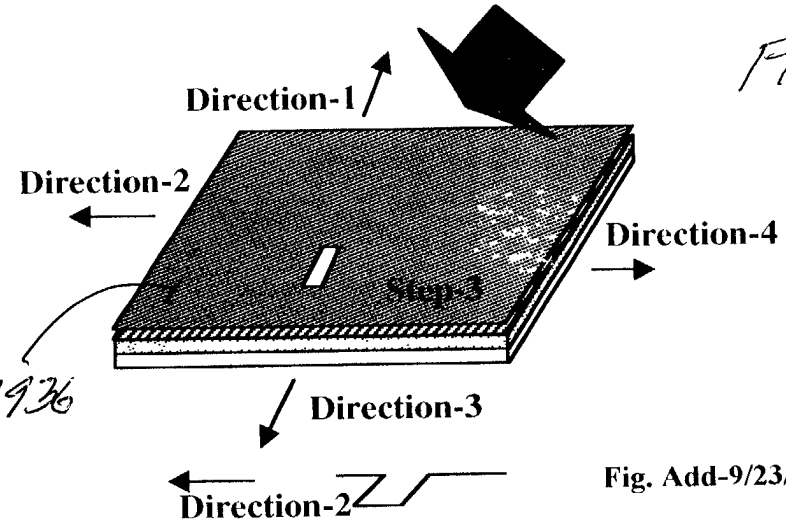


Fig. Add-9/23/99-10

Another Process Flow for Structure (II)

Fig 350

Buffer/Clad/Core/Clad Mask formation For Waveguide/Coupler

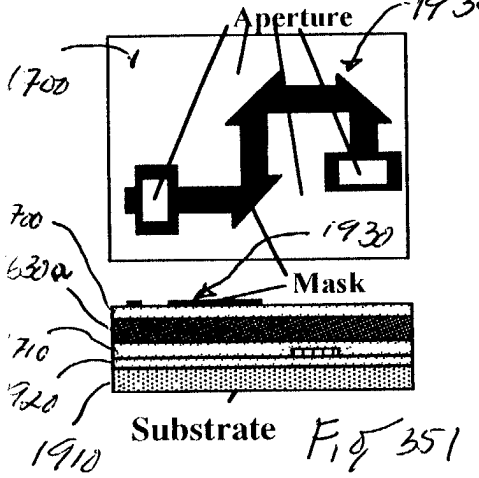


Fig 351

Waveguide Formation MNA or MNE

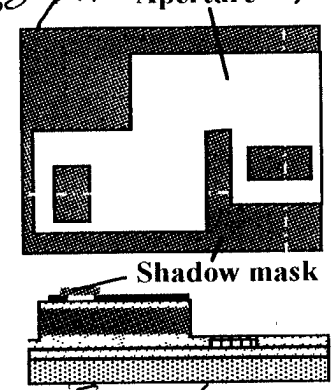


Fig 355 Fig 356

Coupler Formation I MNA or MNE

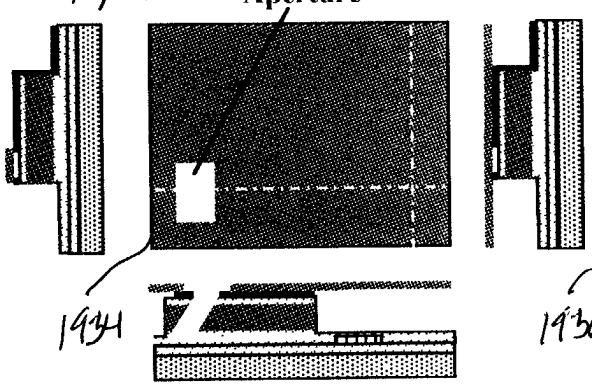


Fig 357 Fig 361 Fig 362

Coupler Formation II MNA or MNE

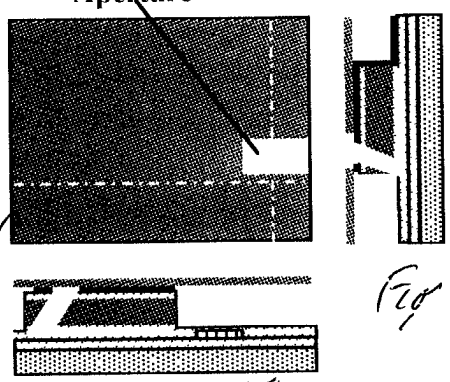


Fig 363 Fig 367 Fig 368 Fig 369

(MNA: Moving Neon Ablation)
(MNE: Moving Neon Etching)

Mask Removal/ Metal or Diclectric Filteror Other materials Depo

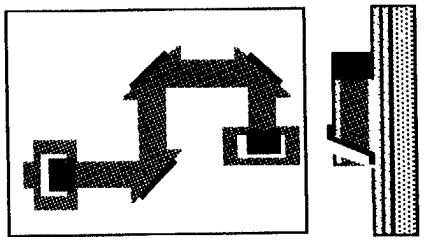


Fig 352 Fig 353

Clad

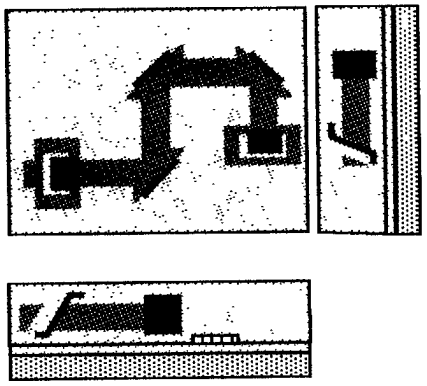


Fig 354 Fig 358 Fig 359 Fig 360

Metallization

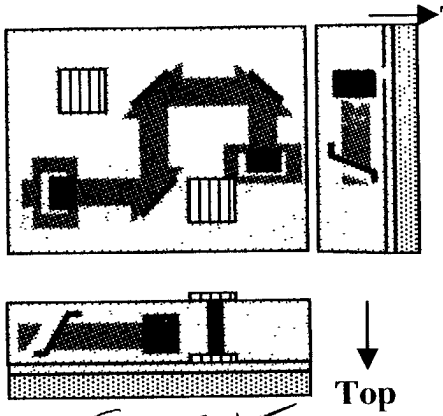


Fig 364 Fig 365 Fig 366

Z-Connection Substrate Removal

Fig. Add-9/23/99-9

Excimer Laser Ablation Example for Beveled Cut (2)

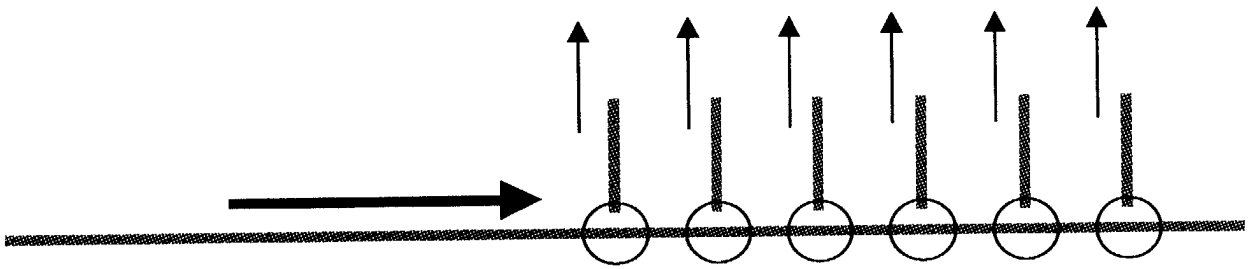


Fig 348

Beam Splitter

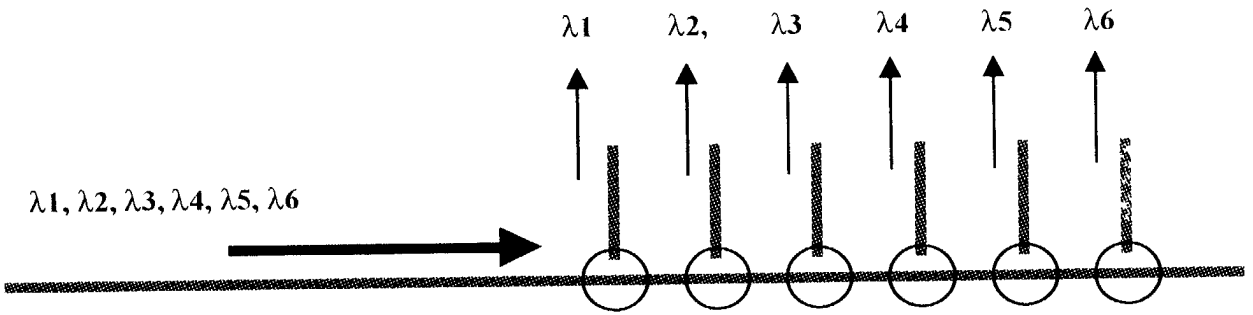


Fig 349

WDM DEMAX

Fig. Add-9/23/99-8

Invented Coupler Structure (II)

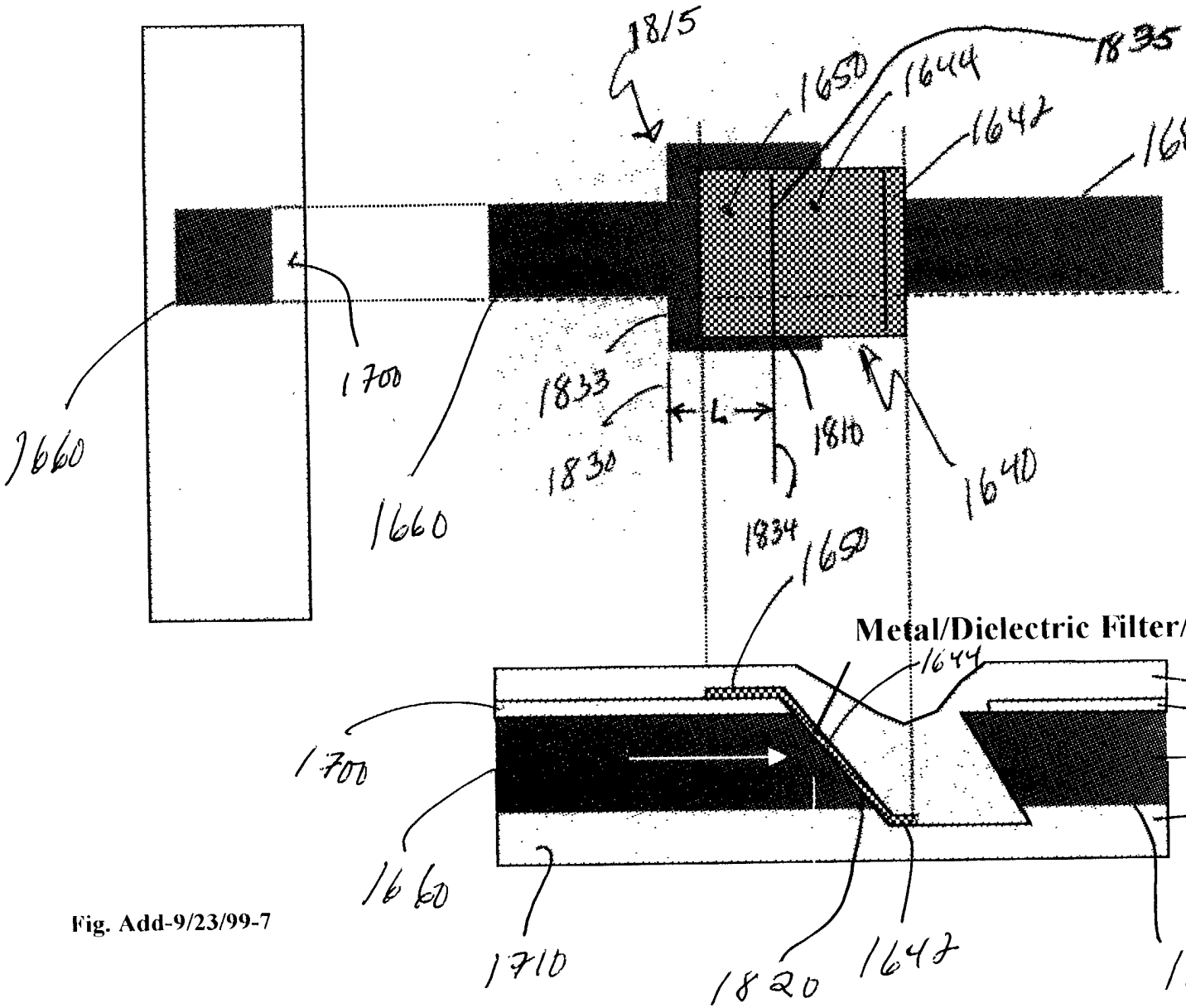


Fig 346

Fig 347

Fig. Add-9/23/99-7

Invented Coupler Structure (I)

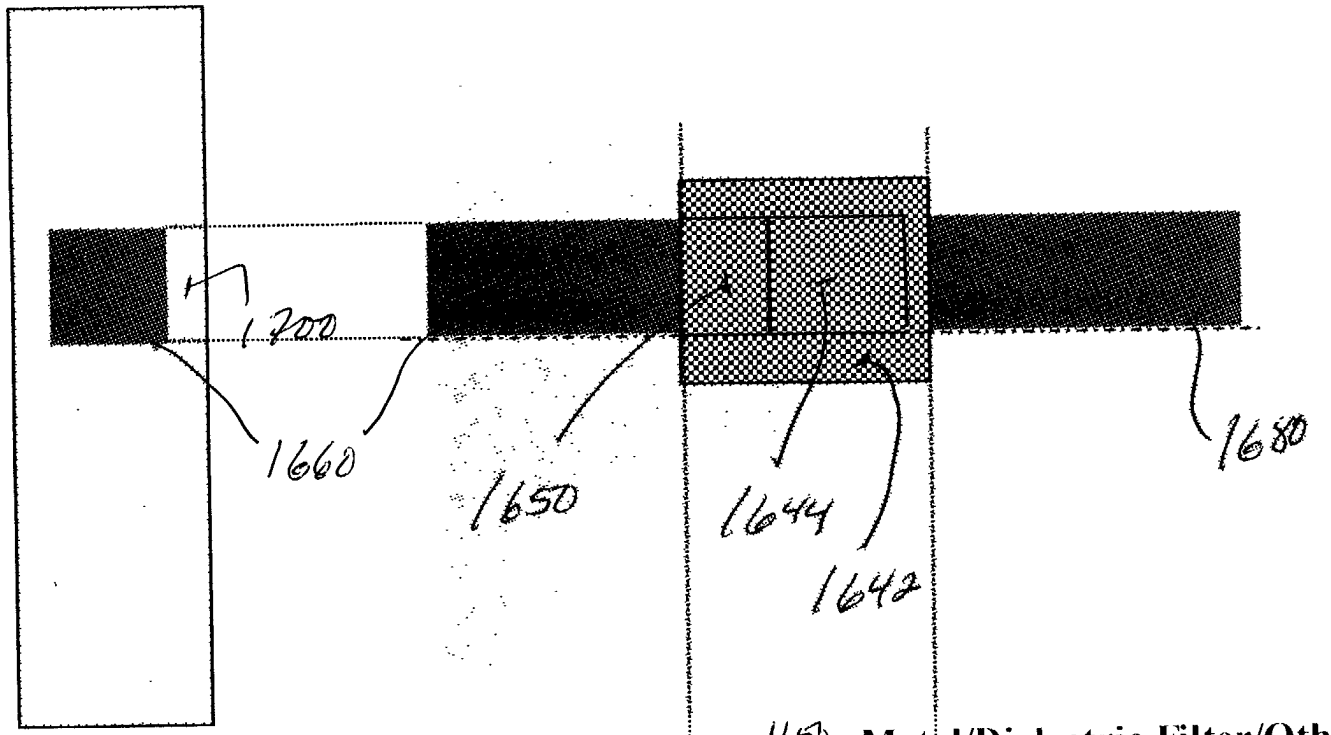


Fig 344

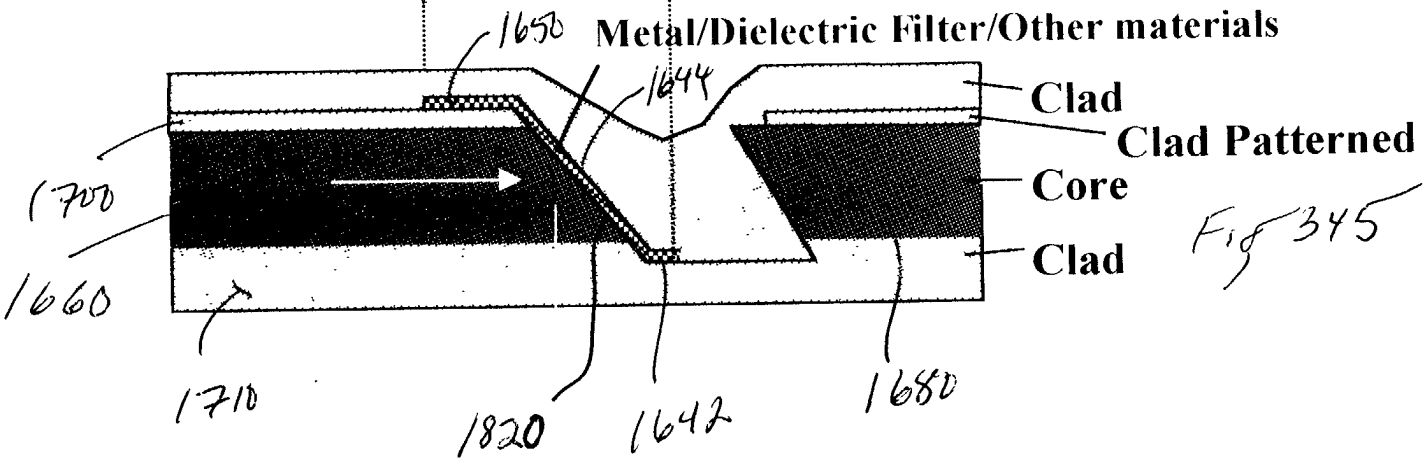


Fig 345

Fig. Add-9/23/99-6

Conventional Coupler Structure (I)

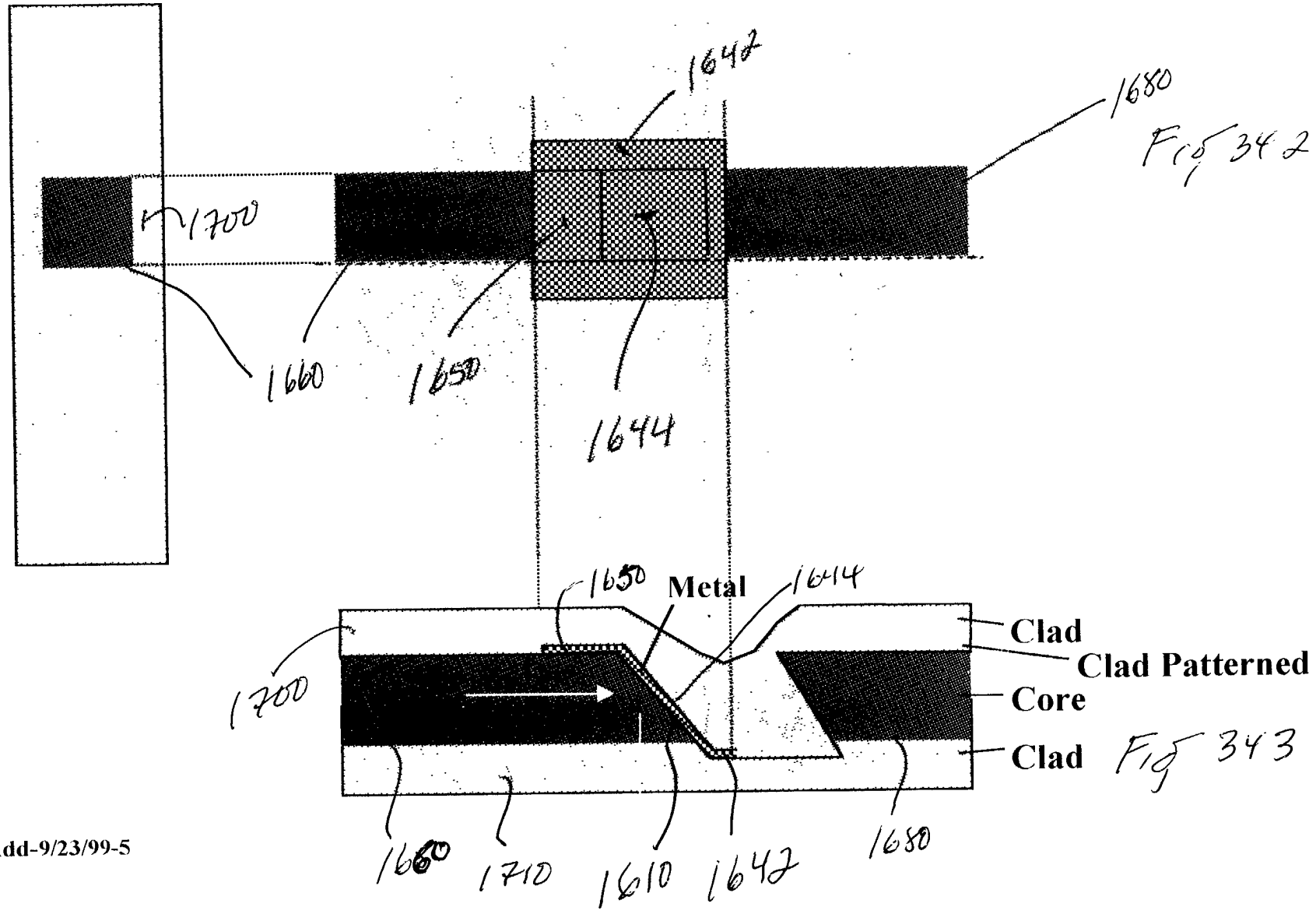


Fig. Add-9/23/99-5

Invented Corner Turning Structure (II)

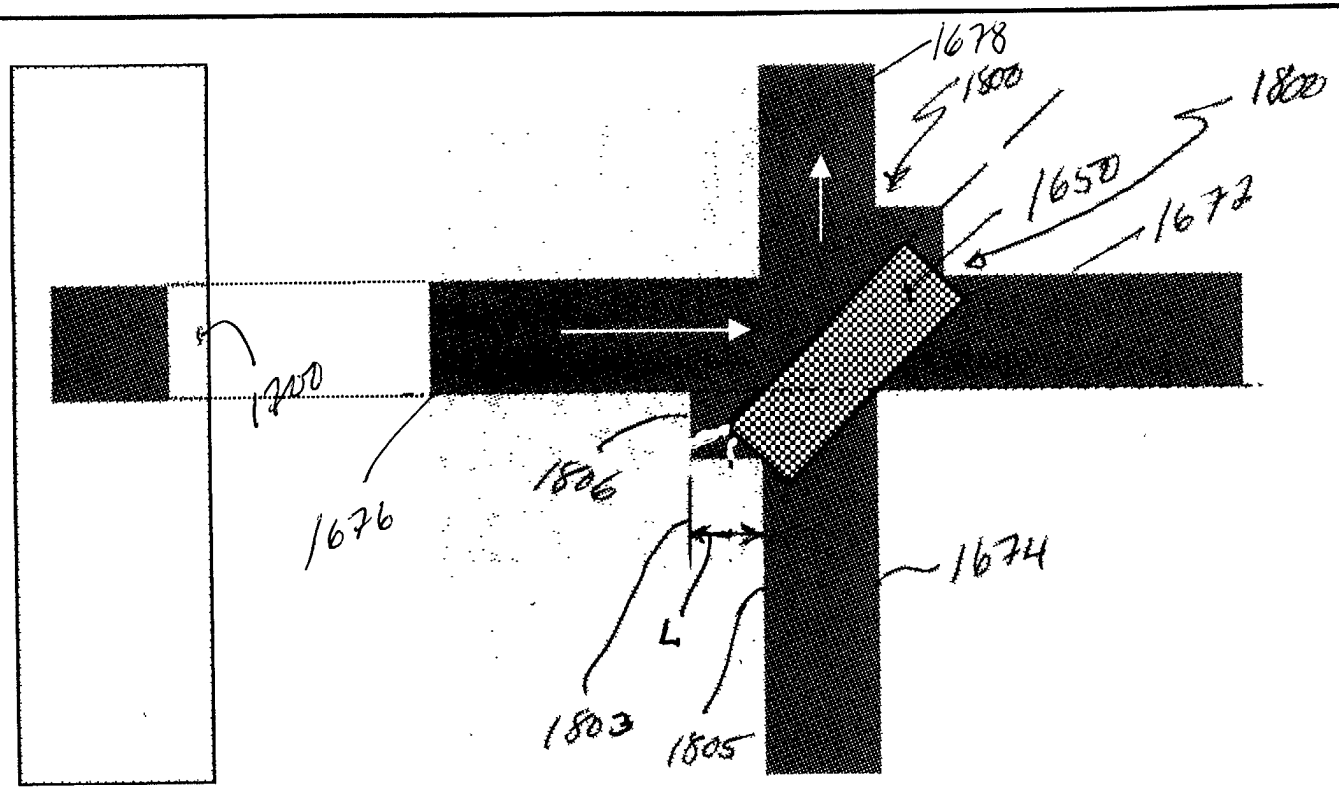


Fig 340

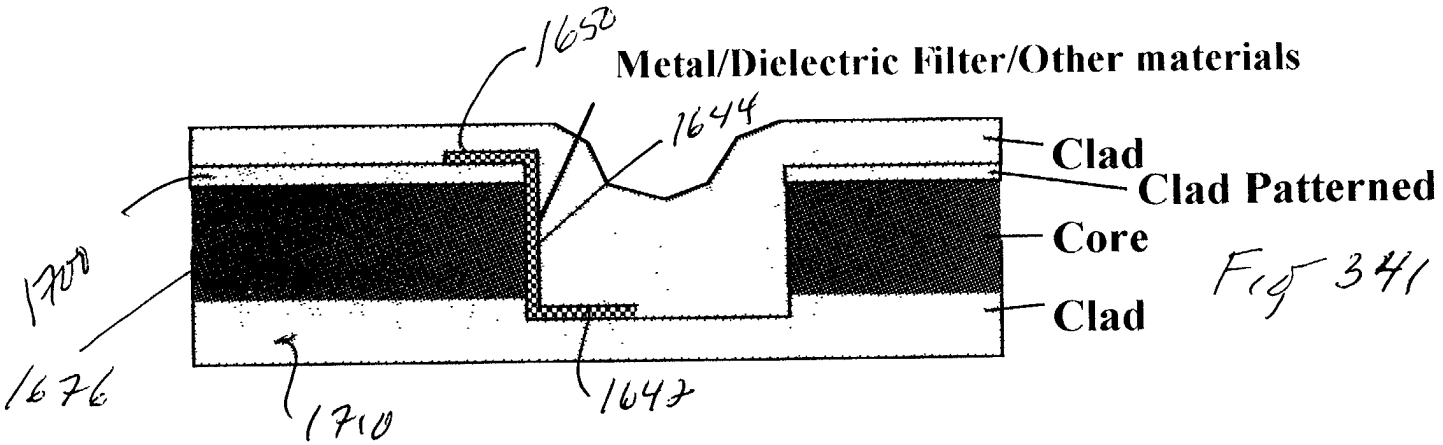


Fig 341

Invented Corner Turning Structure (I)

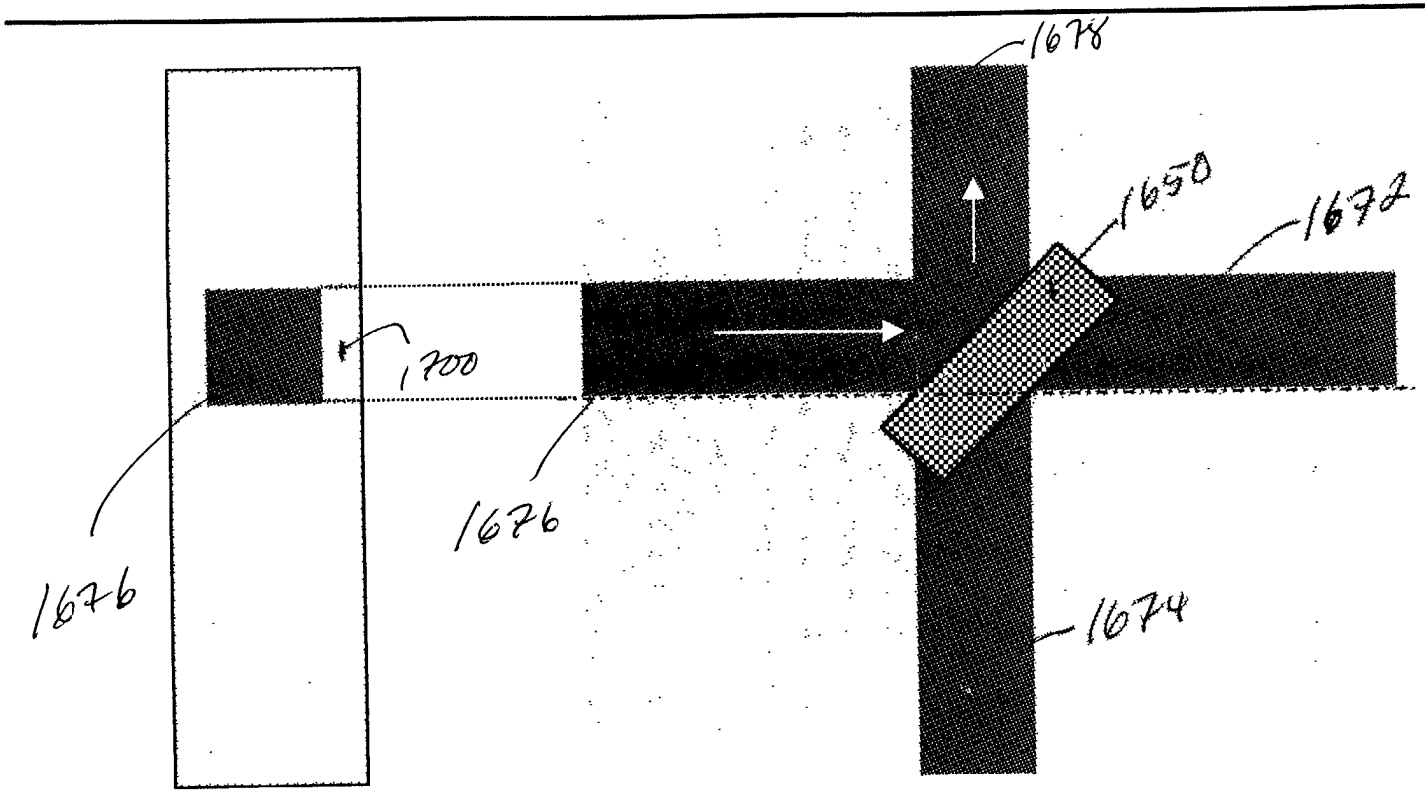


Fig 338

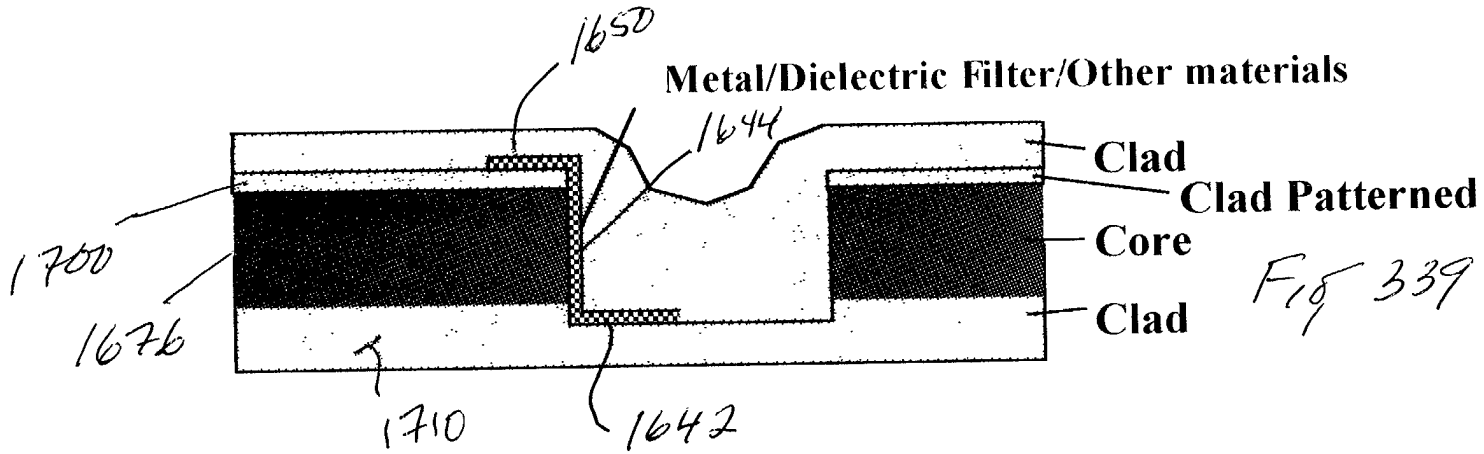


Fig 339

Conventional Corner Turning Structure

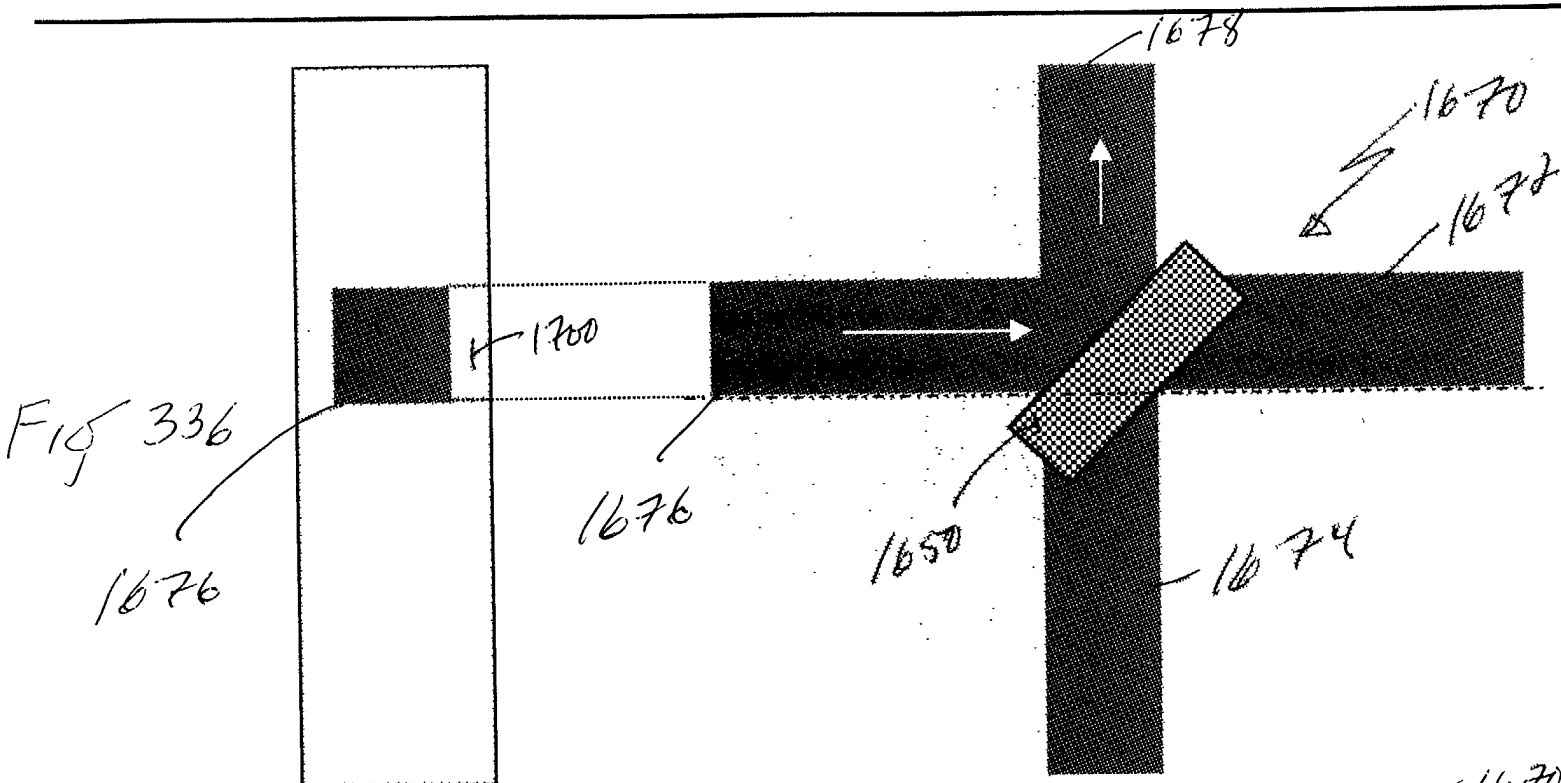


Fig 336

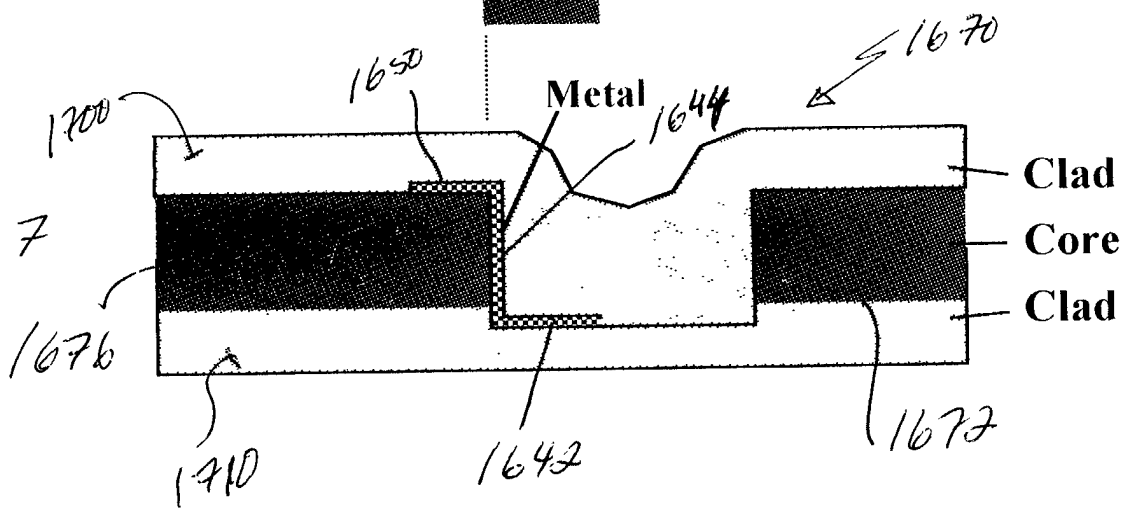
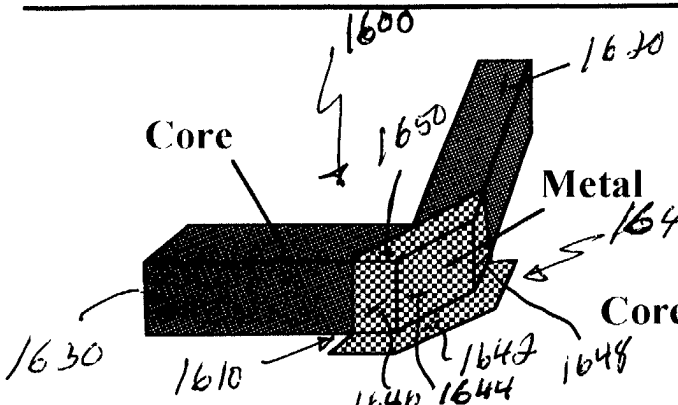


Fig 337

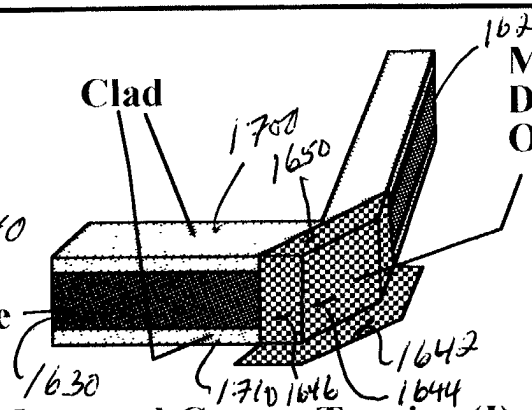
Fig. Add-9/23/99-2

Conventional and Invented Waveguide Structure Examples



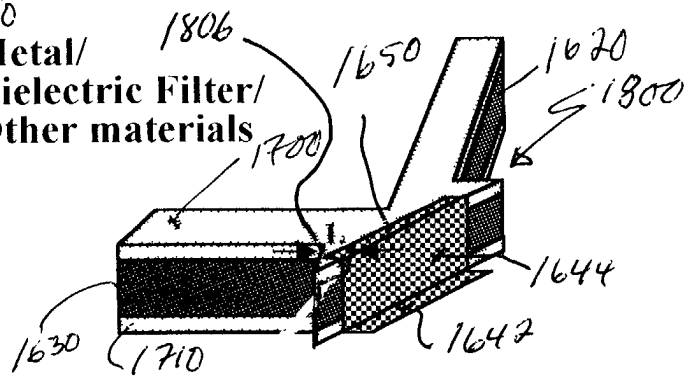
Conventional Corner Turning

Fig 330



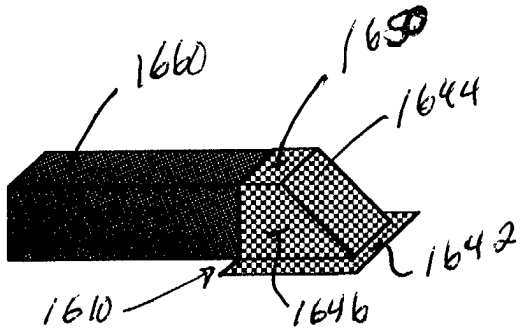
Invented Corner Turning (I)

Fig 332



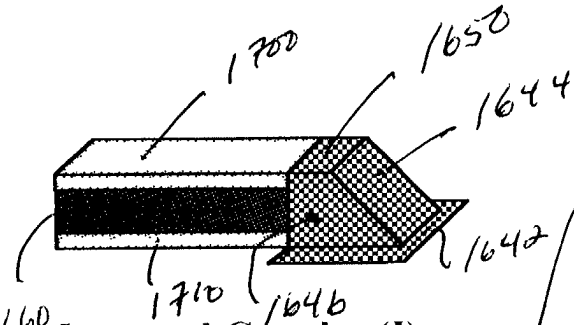
Invented Corner Turning (II)

Fig 334



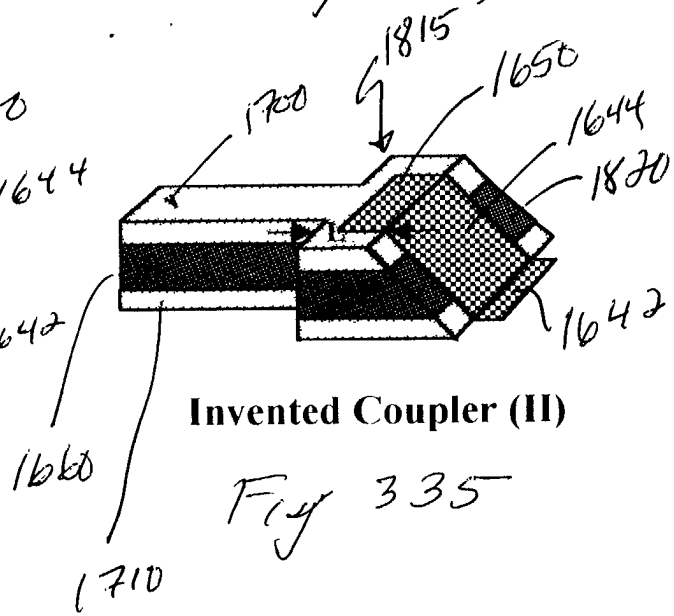
Conventional Coupler

Fig 331



Invented Coupler (I)

Fig 333



Invented Coupler (II)

Fig 335

Fig. Add-9/23/99-1

Example 3: Z waveguide Fab. Process 1

(a1) Metal pattern formation

(a2) Core coat9
[DuPont, AlliedSig , ORMOCERs or F-PI]

(a3) Z-WG core patterning
[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

(a4) Clad coat
(for planarization viscosity adjust if necessary CMP)

(a5) Core coat
[DuPont, AlliedSig , ORMOCERs or F-PI]

(a6) WG core patterning
[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

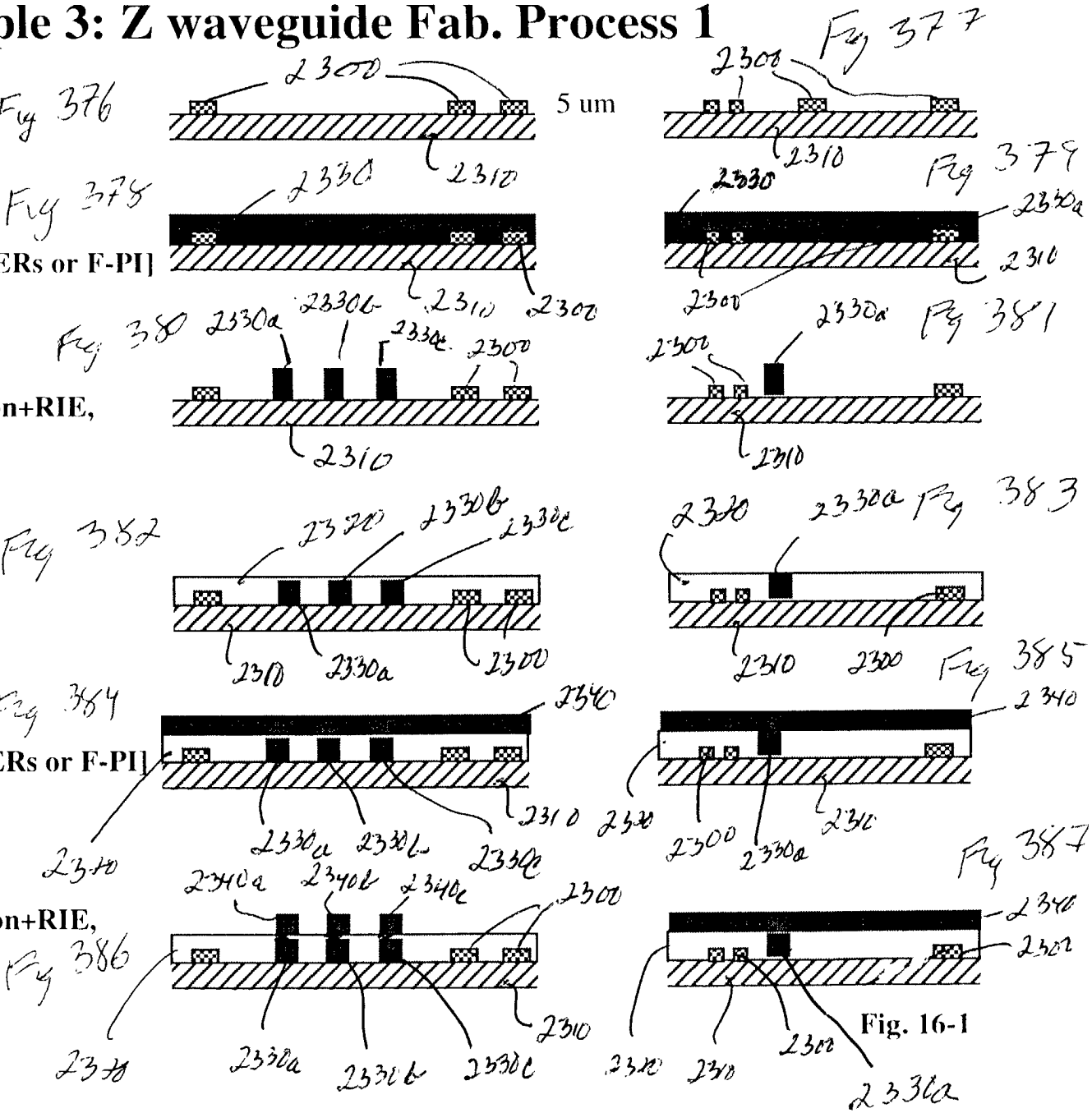


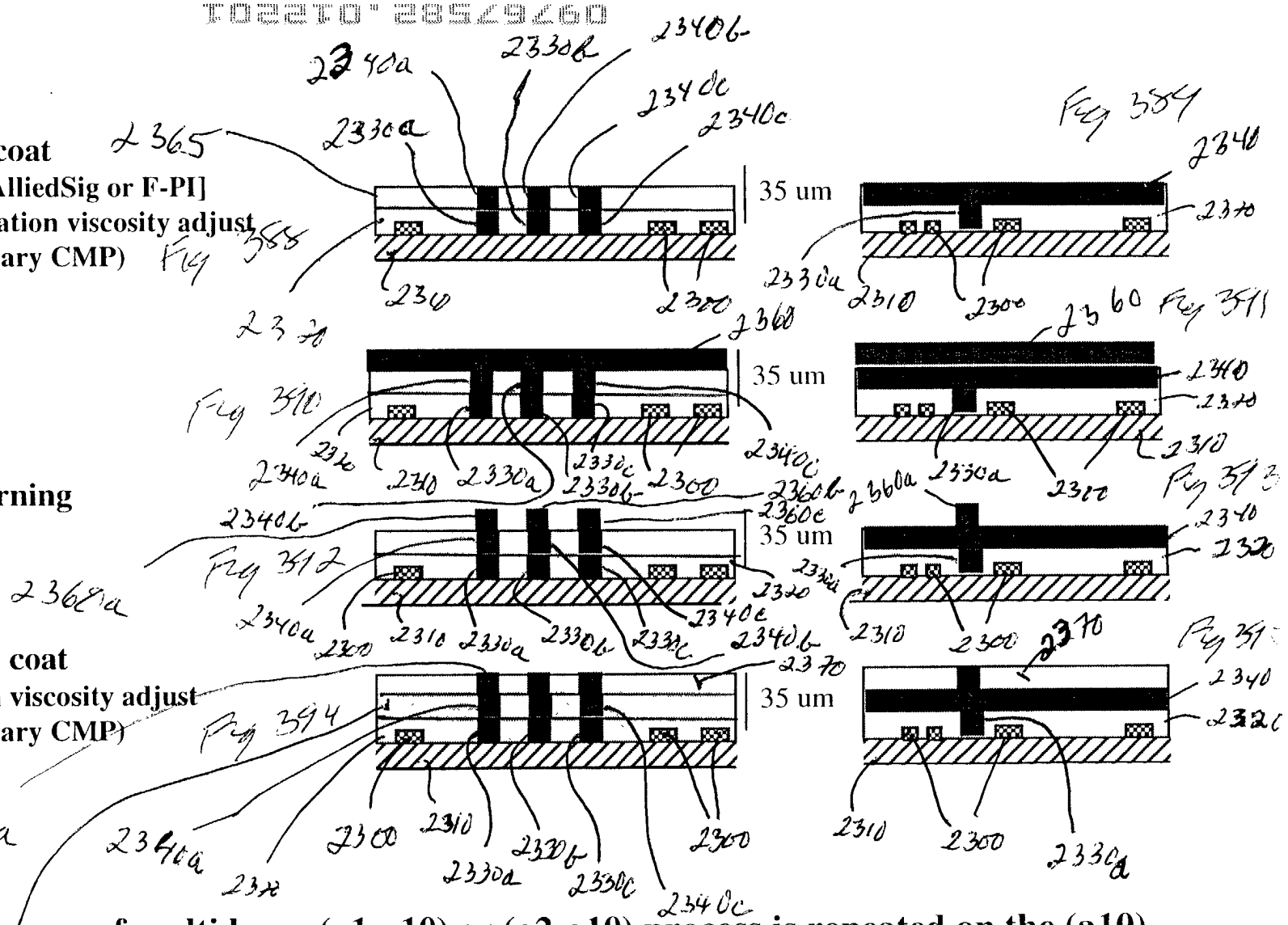
Fig. 16-1

(a7) Over clad coat
[DuPont or AlliedSig or F-PI]
(for planerization viscosity adjust
if necessary CMP)

(a8) Core coat

(a9) Core patterning

(a10) Over clad coat
(for planarization viscosity adjust
if necessary CMP)



In the case of multi layer (a1-a10) or (a2-a10) process is repeated on the (a10).

Fig. 16-2

Example 4: Z waveguide Fab. Process 2

(a1) Metal pattern formation

(a2) Clad coat
[DuPont, AlliedSig , ORMOCERs or F-PI]

(a3) Clad patterning
[UV-Exposure, mask-formation+RIE, Laser or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

(a4) Core coat
(for planarization viscosity adjust if necessary CMP)

(a5) WG core patterning
[UV-Exposure, mask-formation+RIE, Laser or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

(a6) Over clad coat
[DuPont or AlliedSig or F-PI]
(for planerization viscosity adjust if necessary CMP)

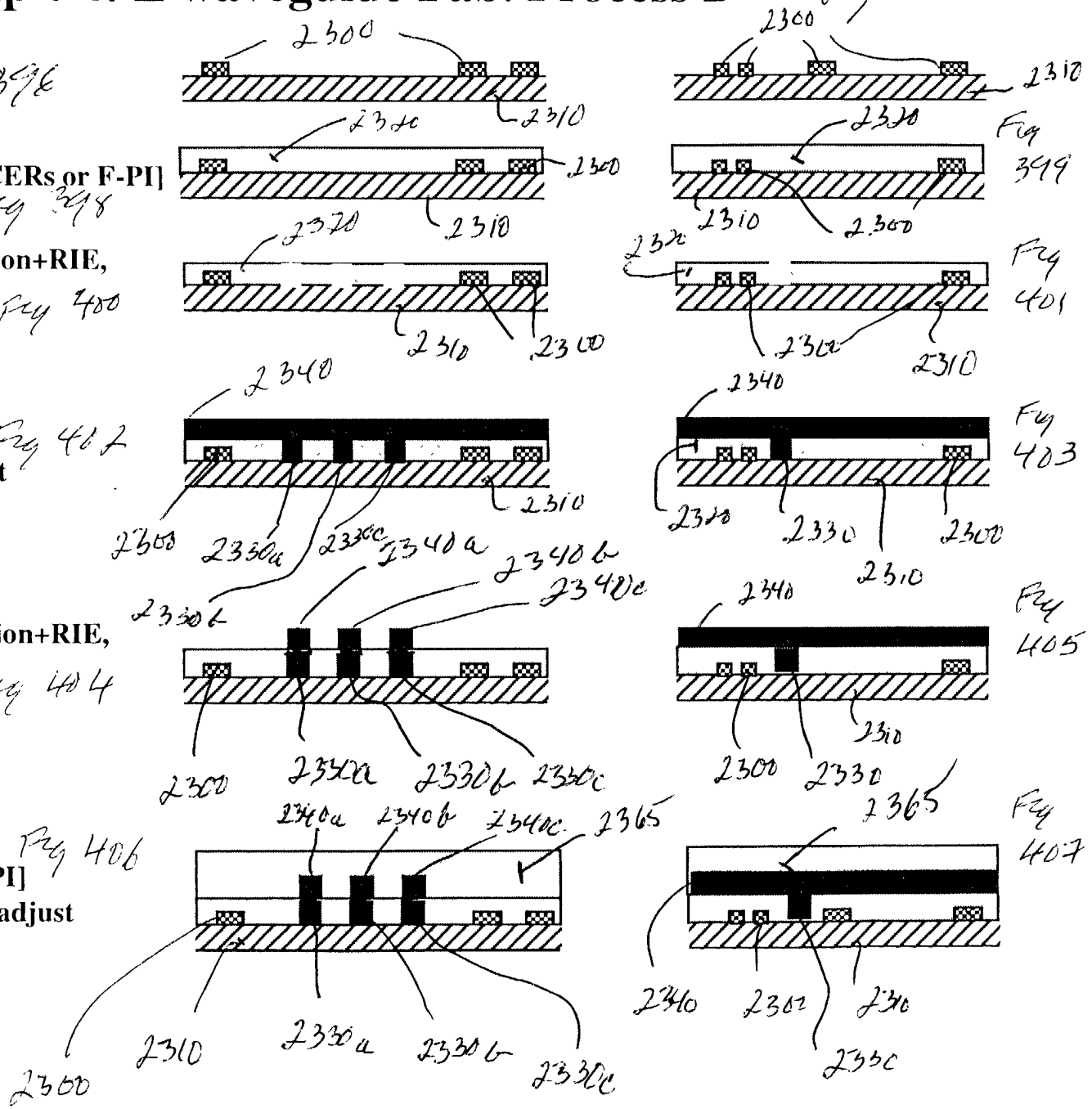


Fig. 17-1

(a7) Clad patterning

[UV-Exposure, mask-formation+RIE, Laser or Dupont process]

Develpment

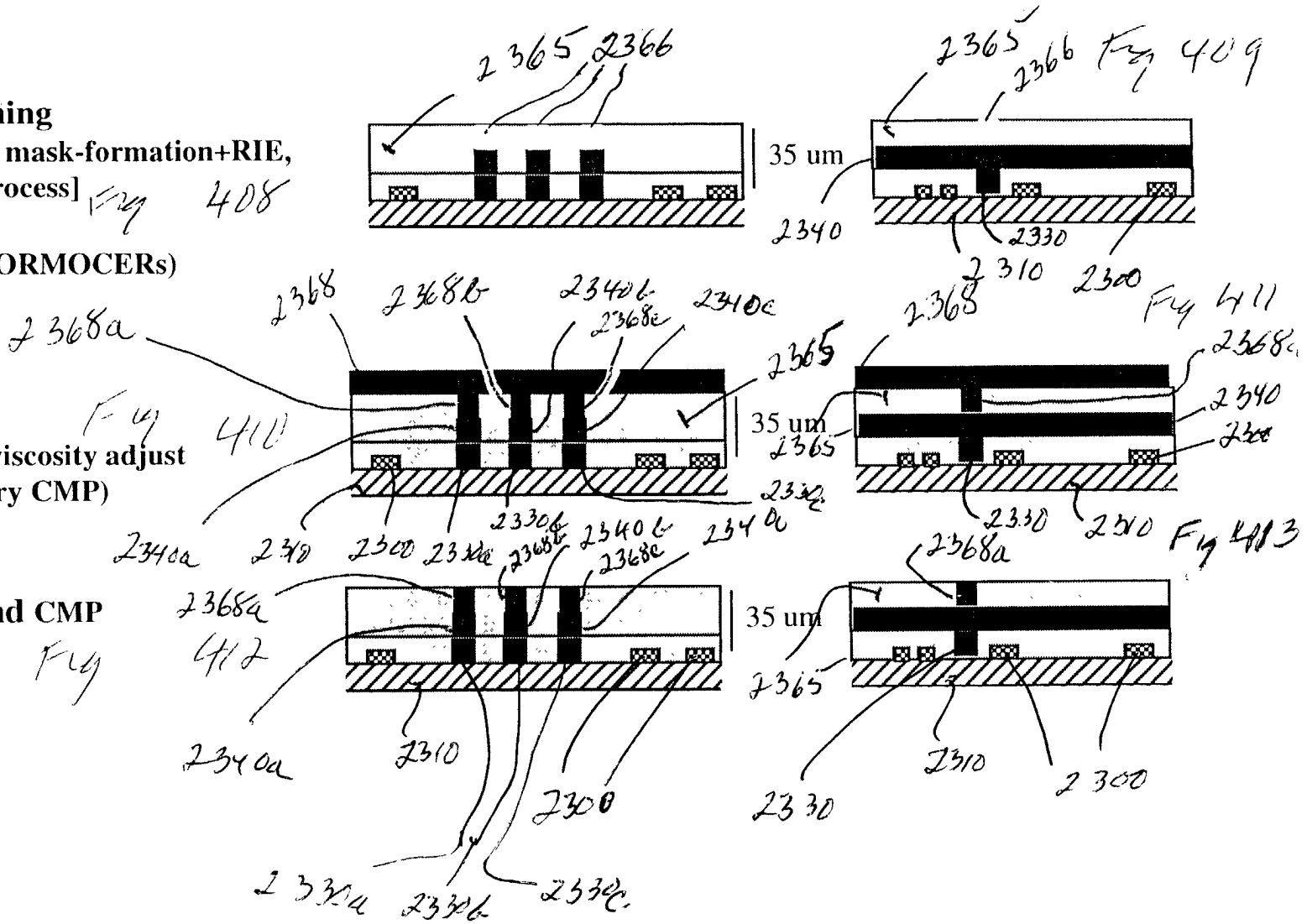
(for AlliedSig, ORMOCERs)

(a8) Core coat

(for planarization viscosity adjust if necessary CMP)

or

(a8) Core coat and CMP



In the case of multi layer (a1, a5-a8) or (a5-a8) process is repeated on the (a8).

Fig. 17-2

Fig. 414

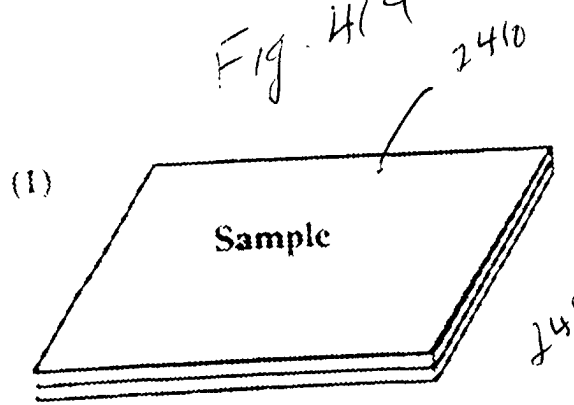


Fig. 415

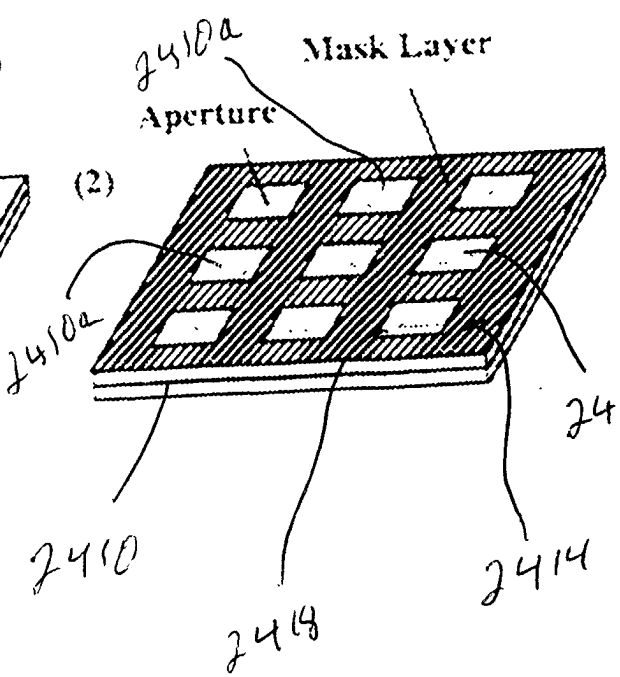
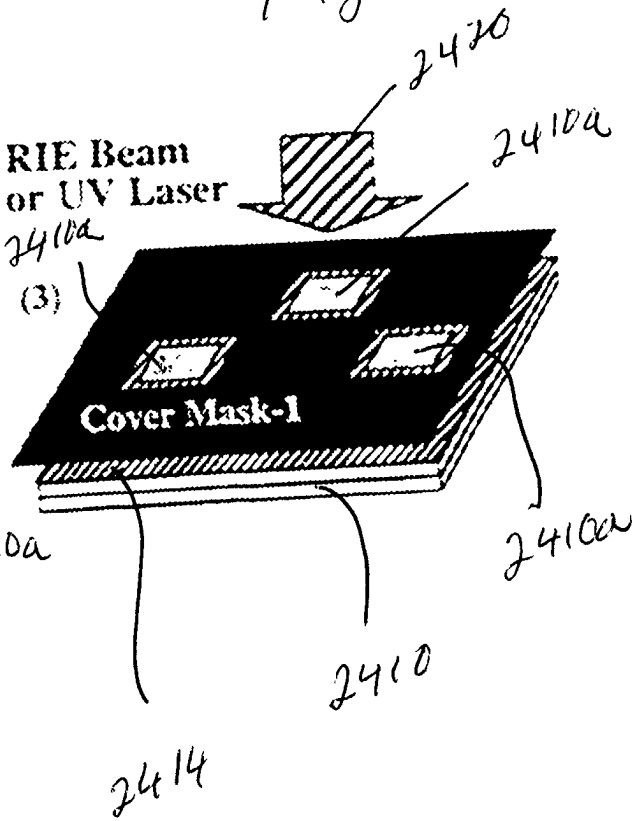
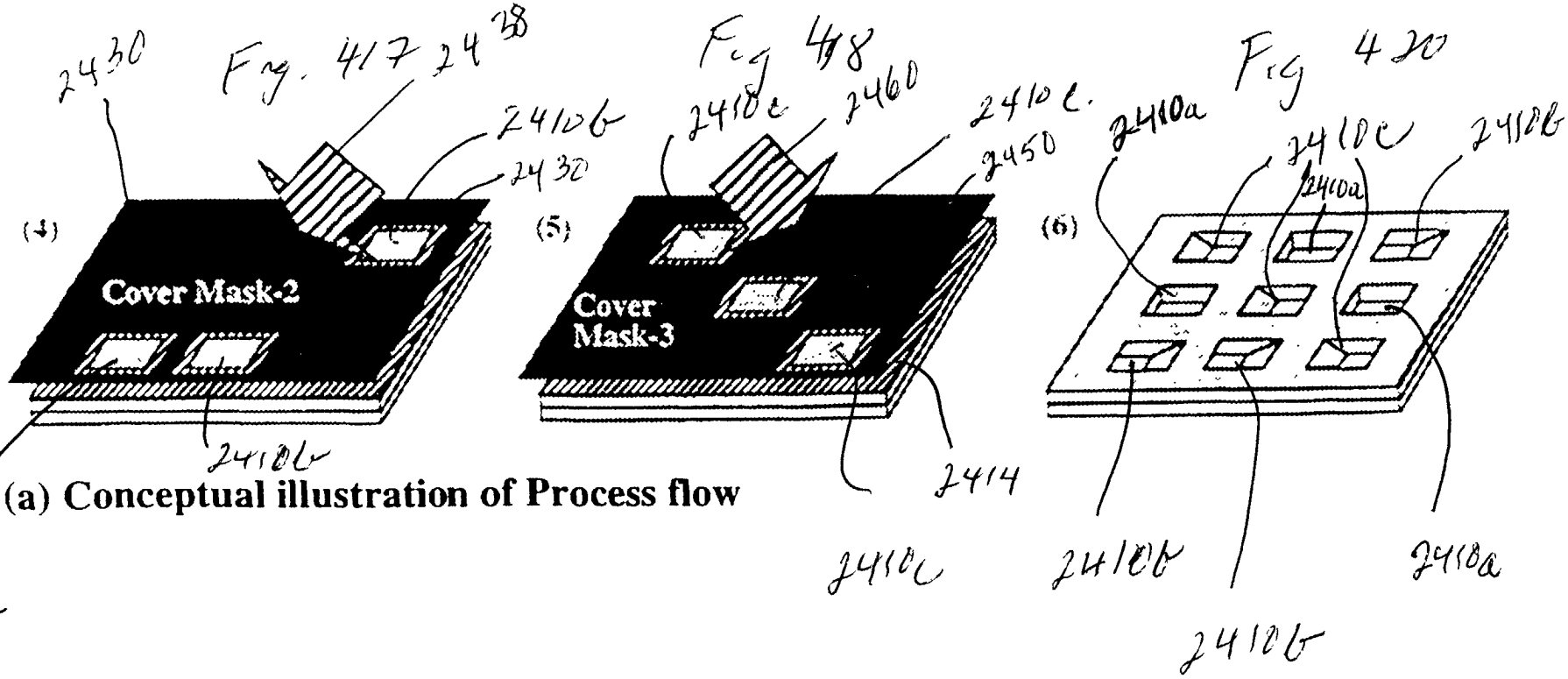


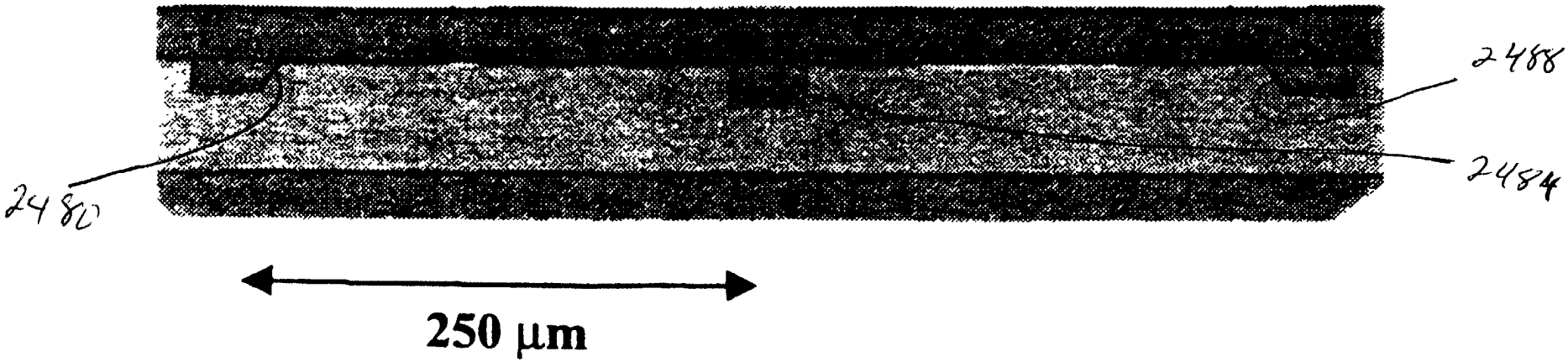
Fig. 416





(a) Conceptual illustration of Process flow

Fig. 421



(b) Trench wall formation of three different angles